# MA5721 Datasheet
# 2.4MHz 1A Step-Down Converter with I2C Interface

**Version:** **0.8**
**Release date:** **2023-07-11**

# Version History

| Version | Date | Description |
|---|---|---|
| 0.8 | 2023-07-11 | Absolute Maximum Ratings on P11<br>Recommended Operating Conditions on P11<br>Thermal Information on P12<br>Add note in chapter 4.2 on P12<br>Add note in chapter 4.3 on P12<br>Add note in chapter 4.4 on P13<br>Add note in Table 4-2 on P14 |

# Table of Contents

## List of Figures



## List of Tables

# 1 Overview

## 1.1 General Description

The MA5721 is a step-down switching voltage regulator that delivers a digitally programmable output from an input voltage supply of 2.5V to 5.5V. The output voltage is programmed through an I2C interface capable of operating up to 3.4MHz.

Using a proprietary architecture with synchronous rectification, the MA5721 is capable of delivering 1A continuously at over 80% efficiency, maintaining that efficiency at load currents as low as 10mA. The regulator operates at a nominal fixed frequency of 2.4MHz, which reduces the value of the external components. Additional output capacitance can be added to improve regulation during load transients without affecting stability.

At moderate and light loads, Pulse Frequency Modulation (PFM) is used to operate in Power-Save Mode with a typical quiescent current of 45µA at room temperature. Even with such a low quiescent current, the part exhibits excellent transient response during large load swings. At higher loads, the system automatically switches to fixed- frequency control, operating at 2.4MHz. In the Shutdown Mode, the supply current drops below 1µA, reducing power consumption. The PFM Mode can be disabled if fixed frequency is desired. The MA5721 is available in a small WL-CSP-11B 1.31x1.62 (BSC).

## 1.2 Features

- Steady 2.4MHz Switching Frequency
- Continuous Output Current Capability : 1A
- 2.5V to 5.5V Input Voltage Range
- Digitally Programmable Output Voltage
  - 0.3V to 1.3V Programmable Slew Rate for Voltage Transitions
- $I^2C$-Compatible Interface Up to 3.4MHz
- PFM Mode for High Efficiency in Light Load
- Quiescent Current in PFM Mode : 45µA (Typical)
- Input Under-Voltage Lockout (UVLO)
- Thermal Shutdown and Overload Protection
- Power Good Indicator

## 1.3 Applications

- Wearable and Portable Electronic Devices
- DDR Memories, LPDDR3, LPDDR4, LPDDR5
- Tablets, Netbooks, Ultra-Mobile PCs
- Smart Speakers, Voice Assistant Devices
- TV Stick, OTT and Home Entertainment Devices
- Industrial HMI, desktop POS, KIOSK, digital signage

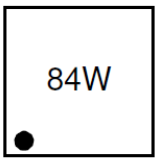
## 1.4 Ordering Information

*Table 1-1. Ordering options*

| Product | MTK Item | Power-Up Defaults | | EN Delay Time | Package Type |
|---|---|---|---|---|---|
| | | VSEL0 | VSEL1 | | |
| MA5721AWSC | MA5721AP/A | 0.9V | 0.8V | 0ms | WL-CSP-11B 1.31x1.62 (BSC) |
| MA5721BWSC | MA5721BP/B | 0.9V | 1.05V | 6ms | |
| MA5721CWSC | MA5721CP/A | 0.6V | 0.4V | 6ms | |
| MA5721DWSC | MA5721DP/A | 1.125V | 1.125V | 3ms | |
| MA5721EWSC | MA5721EP/A | 0.8V | 0.75V | 3ms | |
| MA5721FP/A | MA5721FP/A | 0.75V | 0.75V | 0ms | |

## 1.5 Marking Information

MA5721AP/A

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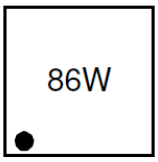
MA5721DP/A

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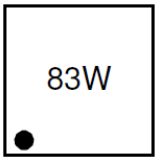


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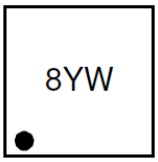
MA5721EP/A

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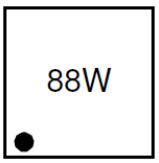


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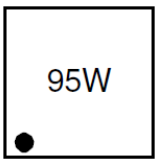


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## 1.6 Pin Configuration

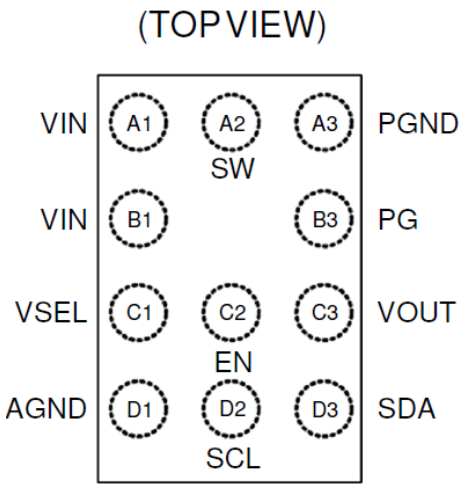



***Figure 1-1. WL-CSP-11B 1.31x 1.62 (BSC)***

***Table 1-2. Functional Pin Description***

| Pin No. | Pin Name | Pin Function |
|---|---|---|
| A1, B1 | VIN | Power input voltage. Connect to the input power source. Connect to $C_{IN}$ with minimal path. |
| A2 | SW | Switching node. Connect to the inductor. |
| A3 | PGND | Power ground. The low-side MOSFET is referenced to this pin. $C_{IN}$ and $C_{OUT}$ should be returned with a minimal path to these pins. |
| B3 | PG | Power good indicator. The output of this pin is an open-drain with external pull-up resistor. After soft startup, PG is pulled up when the FB voltage is within 87% (typ.). The PG status is low while EN is disabled. Note that when VIN is lower than 2.32V (typ.), the PG pin will keep low to indicate the power is not ready. |
| C1 | VSEL | Voltage select. When this pin is low, $V_{OUT}$ is set by the VSEL0 register. When this pin is high, $V_{OUT}$ is set by the VSEL1 register. Polarity of this pin in conjunction with the mode bits in the Control register 02h will select Forced PWM or Auto PFM/PWM mode of operation. |
| C2 | EN | Enable control input. A logic-high enables the converter; a logic-low forces the device into shutdown mode, and will reset all registers to the default value. |
| C3 | VOUT | VOUT. Output voltage sense through this pin. Connect to output capacitor. |
| D1 | AGND | Analog ground. All signals are referenced to this pin. Avoid routing high dV/dt AC currents through this pin. |
| D2 | SCL | $I^2C$ serial clock. |
| D3 | SDA | $I^2C$ serial data. |

# 2 Functional Descriptions

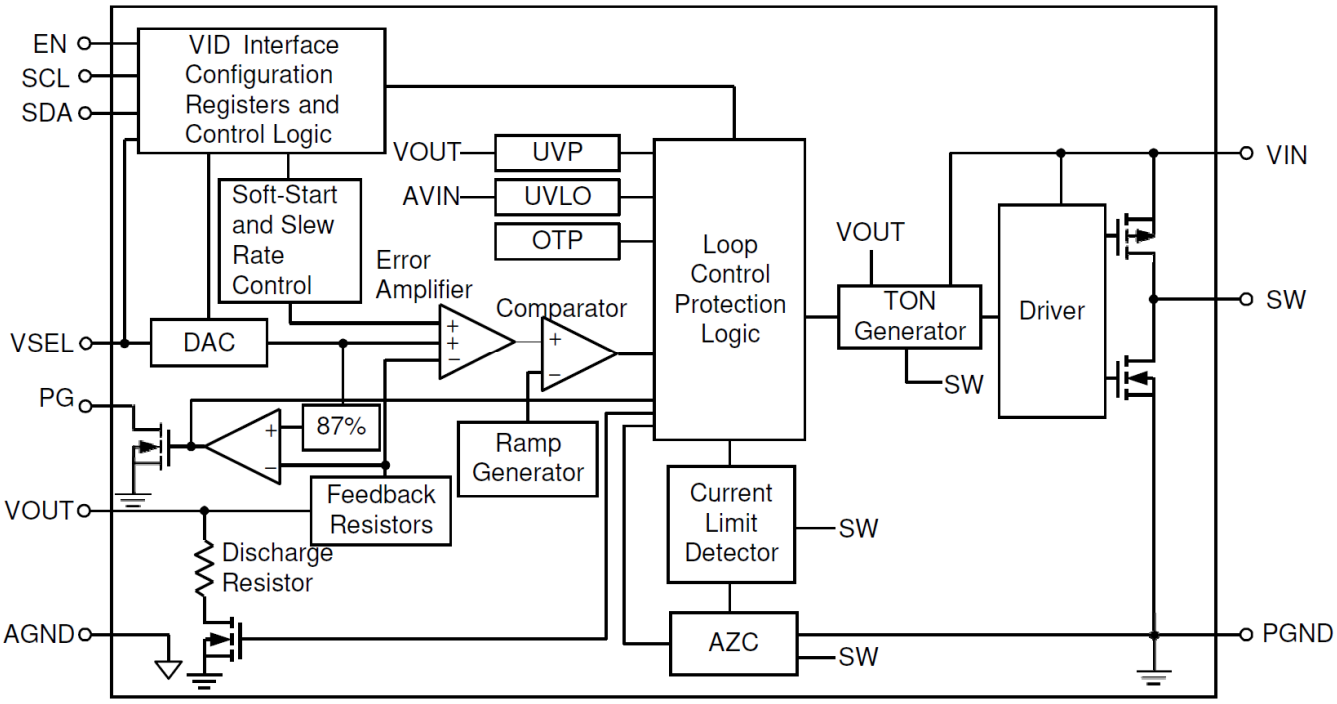



***Figure 2-1. Functional Block Diagram***

# 3 Operation

The MA5721 is a low voltage synchronous step-down converter that supports input voltage ranging from 2.5V to 5.5V and the output current can be up to 1A. The MA5721 uses ACOT®mode control. To achieve good stability with low-ESR ceramic capacitors, the ACOT® uses a virtual inductor current ramp generated inside the IC. This internal ramp signal replaces the ESR ramp normally provided by the output capacitor's ESR. The ramp signal and other internal compensations are optimized for low-ESR ceramic output capacitors.
In steady-state operation, the feedback voltage, with the virtual inductor current ramp added, is compared to the reference voltage. When the combined signal is less than the reference, the on-time one-shot is triggered, as long as the minimum off-time one-shot is cleared and the measured inductor current (through the synchronous rectifier) is below the current limit. The on-time one-shot turns on the high-side switch and the inductor current ramps up linearly. After the on-time, the high-side switch is turned off and the synchronous rectifier is turned on and the inductor current ramps down linearly. At the same time, the minimum off-time one-shot is triggered to prevent another immediate on-time during the noisy switching time and allows the feedback voltage and current sense signals to settle. The minimum off-time is kept short so that rapidly-repeated on-times can raise the inductor current quickly when needed.

## 3.1 PWM Frequency and Adaptive On-Time Control

The on-time can be roughly estimated by the equation :

$$T_{ON} = \frac{V_{OUT}}{V_{IN}} \times \frac{1}{f_{SW}}$$

where $f_{SW}$ is nominal 2.4MHz.

## 3.2 Auto-Zero Current Detector

The auto-zero current detector circuit senses the SW waveform to adjust the zero current threshold voltage. When the current of low-side MOSFET decrease to the zero current threshold, the low-side MOSFET turns off to prevent negative inductor current. In this way, the zero current threshold can be adjusted for different conditions to get better efficiency.

## 3.3 Under-Voltage Protection (UVLO)

The UVLO continuously monitors the voltage of VIN to make sure the device works properly. When the VCC is high enough to reach the high threshold voltage of UVLO, the step-down converter softly starts or pre-biases to its regulated output voltage. When the VIN decreases to its low threshold (160mV hysteresis), the device will shut down.

## 3.4 Power Good Indication Pin

The MA5721 features an open-drain power-good output (PG) to monitor the output voltage status. The output delay of comparator prevents false flag operation for short excursions in the output voltage, such as during line and load transients. Pull-up PG with a resistor to $V_{OUT}$ or an external voltage below 5.5V. When $V_{IN}$ voltage rises above $V_{UVLO}$, the power-good function is activated. After soft- start is finished, the PG pin is controlled by a comparator connected to the feedback signal

$V_{OUT}$. If $V_{OUT}$ rises above a power-good high threshold ($V_{TH\_PGLH}$) (typically 87% of the reference voltage), the PG pin will be in high impedance and $V_{PG}$ will be held high. Moreover, when $V_{IN}$ is above UVLO and device is powered on through EN pin, the PG pin will assert high within 300µs as soon as the $V_{EN}$ is above logic-high threshold; in other words, the PG delay time is around 300µs from EN asserts to logic-high. When $V_{OUT}$ falls below the power-good low threshold ($V_{TH\_PGHL}$) (typically 77% of the reference voltage), the PG pin will be pulled low after a certain delay (3µs, typically). Once being started-up, if any internal protection is triggered, PG will be pulled low to GND. The internal open-drain pull down device (11∧, typically) will pull the PG pin low. The power good indication profile is shown in Table 3-1. Note that when $V_{IN}$ is lower than 2.32V (typically), the PG pin will keep low to indicate the power is not ready.

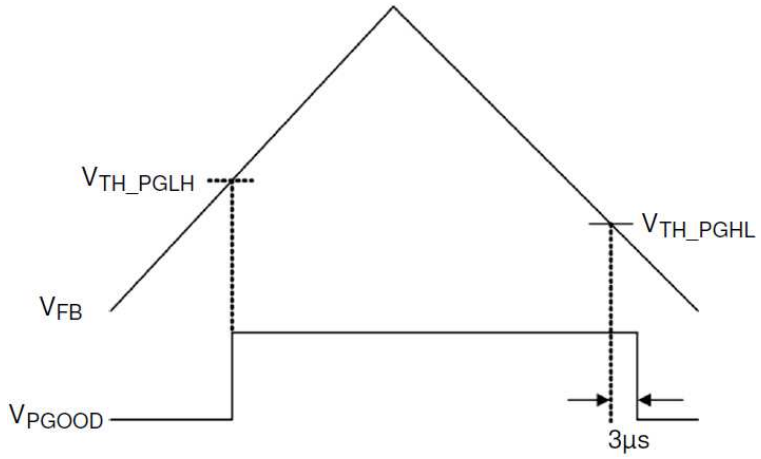



***Figure 3-1. The Logic of PG***

***Table 3-1. PG Pin Status***

| Conditions | | PG Pin |
|---|---|---|
| Enable | $V_{EN} > V_{EN\_H}$, $V_{FB} > V_{TH\_PGLH}$ | High Impedance |
| | $V_{EN} > V_{EN\_H}$, $V_{FB} < V_{TH\_PGHL}$ | Low |
| Shutdown | $V_{EN} < V_{EN\_L}$ | Low |
| OTP | $T_J > T_{SD}$ | Low |

## 3.5 Over-Current Protection (OCP)

When the output voltage of the MA5721 is lower than 59% of the reference voltage after soft-start, the UVP is triggered. The MA5721 senses the current signal when high-side and low-side MOSFET turns on. As a result, the OCP is cycle-by-cycle limit. If the OCP occurs, the converter holds off the next pulse and turns on low-side switch until inductor drops below the valley current limit, and then turns on high-side again to maintain output voltage and supports loading current to output before triggering UVP.

If the OCP condition keeps and the load current is larger than the current which converter can provide, the output voltage will decrease and drop below UVP threshold, and the converter will keep switching for 16 consecutive cycles before entering hiccup operation. The converter latches off 1.7ms when the output voltage is still lower than UVP threshold, and the soft-start sequence begins again after latching off time.

## 3.6 Soft-Start

An internal current source charges an internal capacitor to build the soft-start ramp voltage. The typical soft-start time can be programming by $I^2C$.

## 3.7 Over-Temperature Protection (OTP)

The MA5721 has over-temperature protection. When the device triggers the OTP, the device shuts down.

## 3.8 Over-Voltage Behavior (OV)

The MA5721 provides a natural over-voltage protection function to prevent damage behavior during heavy load released scenario.
When device is set at auto PFM/PWM operation, the high- side and low-side MOSFET will automatically turn off immediately as long as output voltage rises above internal reference target. When the output voltage goes below the target, the internal comparator will trigger on-time controller to resume switching behavior to maintain excellent regulation.
When device is configured as FCCM operation mode, the high-side and low-side MOSFET will continuously switch to regulate the output voltage back to target setting.

# 4 Electrical Characteristics

## 4.1 Absolute Maximum Ratings

Supply Input Voltage, VIN ..... –0.3V to 7V
SW Pin Switch Voltage ..... –0.3V to 7.3V
<50ns ..... –5V to 8.5V
Other I/O Pin Voltages ..... –0.3V to 7.3V
Junction Temperature ..... 150°C
Lead Temperature (Soldering, 10 sec.) ..... 260°C
Storage Temperature Range ..... –65°C to 150°C

**Note:**
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device.
These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions may affect device reliability.

## 4.2 ESD Ratings

- ESD Susceptibility
  HBM (Human Body Model) ..... 2kV

**Note:**
Devices are ESD sensitive. Handling precautions are recommended.

## 4.3 Recommended Operating Conditions

Supply Input Voltage, VIN ..... 2.5V to 5.5V
Junction Temperature Range ..... –40°C to 125°C

**Note:**
The device is not guaranteed to function outside its operating conditions.

## 4.4 Thermal Information

*Table 4-1. Thermal Information*

| Thermal Parameter | | WL-CSP-11B 1.31x1.62 (BSC) | Unit |
|---|---|---|---|
| $\theta_{JA}$ | Junction-to-ambient thermal resistance (JEDEC standard) | 48.8 | °C/W |
| $\theta_{JC(Top)}$ | Junction-to-case (top) thermal resistance | 18 | °C/W |
| $\theta_{JC(Bottom)}$ | Junction-to-case (bottom) thermal resistance | 4.44 | °C/W |
| $\theta_{JA(EVB)}$ | Junction-to-ambient thermal resistance (specific EVB) | 65.4 | °C/W |
| $\Psi_{JC(Top)}$ | Junction-to-top characterization parameter | 2.2 | °C/W |
| $\Psi_{JB}$ | Junction-to-board characterization parameter | 41.1 | °C/W |

**Note 1:**

For more information about thermal parameter, see the Application and Definition of Thermal Resistances report, AN061.

**Note 2:**

$\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and $\Psi_{JB}$ are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm, furthermore, all layers with 1 oz. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

## 4.5 Electrical Characteristics

*Table 4-2. General electrical specification*

($V_{IN}$ = 3.6V, $T_A$ = 25°C, unless otherwise specified)

| Parameter | | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|---|
| Operating Quiescent Current PWM | | $I_{Q\_PWM}$ | $I_{LOAD}$ = 0, mode Bit = 1 (Forced PWM) | -- | 15 | -- | mA |
| Operating Quiescent Current PFM | | $I_{Q\_PFM}$ | $I_{LOAD}$ = 0 | -- | 45 | -- | µA |
| H/W Shutdown Supply Current | | $I_{SHDN\_H/W}$ | EN = GND | -- | 0.1 | 3 | µA |
| S/W Shutdown Supply Current | | $I_{SHDN\_S/W}$ | EN = $V_{IN}$, 0x06[1:0] = 2'b00, 2.5V ≤ $V_{IN}$ ≤ 5.5V | -- | 2 | 12 | µA |
| Under-Voltage Lockout Threshold | | $V_{UVLO}$ | $V_{IN}$ rising | -- | 2.32 | 2.45 | V |
| Under-Voltage Lockout Hysteresis | | $\Delta V_{UVLO}$ | | -- | 350 | -- | mV |
| High-Side Switch-On Resistance | | $R_{DS(ON)\_H}$ | $V_{IN}$ = 5V | -- | 60 | -- | mΩ |
| Low-Side Switch-On Resistance | | $R_{DS(ON)\_L}$ | $V_{IN}$ = 5V | -- | 34 | -- | mΩ |
| Enable Threshold Voltage | Logic-High | $V_{IH}$ | 2.5V ≤ $V_{IN}$ ≤ 5.5V | 0.74 | 0.9 | 1.06 | V |
| | Logic-Low | $V_{IL}$ | 2.5V ≤ $V_{IN}$ ≤ 5.5V | 0.64 | 0.8 | 0.92 | |

| | | | | | | |
|---|---|---|---|---|---|---|
| Enable Input Bias Current | $I_{EN}$ | EN Pin tied to GND or VIN | -- | 0.01 | 1 | µA |
| VOUT DC Accuracy | | 2.5V ≤ $V_{IN}$ ≤ 5.5V, $V_{OUT}$ from minimum to maximum, $I_{OUT(DC)}$ = 0A to 1A, Auto PFM/PWM (Note 2) | –3 | -- | 5 | % |
| | | 2.5V ≤ $V_{IN}$ ≤ 5.5V, $V_{OUT}$ from minimum to maximum, $I_{OUT(DC)}$ = 0A to 1A, Forced PWM (Note 2) | –1.5 | -- | 1.5 | % |
| Load Regulation | $\Delta V_{LOAD}$ | $I_{OUT(DC)}$ = 0.5A to 1A (Note 2) | -- | 0.1 | -- | %/A |
| Line Regulation | $\Delta V_{LINE}$ | 2.5V ≤ $V_{IN}$ ≤ 5.5V, $I_{OUT(DC)}$ = 1A (Note 2) | -- | 0.2 | -- | %/V |
| Transient Load Response | $AC_{LOAD}$ | $I_{LOAD}$ step 0.01A to 1A, $t_R$ = $t_F$ = 500ns, $V_{OUT}$ = 1.125V (Note 2) | -- | ±45 | -- | mV |
| Transient Load Response | $AC_{LOAD}$ | $I_{LOAD}$ step 0.01A to 0.8A, $t_R$ = $t_F$ = 1µs, L = 0.33µH, $C_{OUT}$ = 22µF x 2 (Note 2) | -- | 45 | -- | mV |
| Line Transient | $V_{LINE}$ | $V_{IN}$ = 3V to 3.6V, $t_R$ = $t_F$ = 10µs, $I_{OUT}$ = 100mA, Forced PWM mode (Note 2) | -- | ±40 | -- | mV |
| High-Side MOSFET Peak Current Limit | $I_{LIM\_P}$ | | -- | 3.15 | -- | A |
| Low-Side MOSFET Valley Current Limit | $I_{LIM\_V}$ | | -- | 1.67 | -- | A |
| Thermal Shutdown | $T_{SD}$ | | -- | 150 | -- | °C |

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| Thermal Shutdown Hysteresis | $\Delta T_{SD}$ | | -- | 15 | -- | °C |
| Switching Frequency | $f_{SW}$ | MA5721A : 0.9V<br>MA5721B : 0.9V<br>MA5721C : 0.6V<br>MA5721D : 1.125V<br>MA5721E : 0.8V<br>MA5721F : 0.75V | 2100 | 2400 | 2700 | kHz |
| Minimum Off-Time | $t_{OFF\_MIN}$ | | -- | 170 | -- | ns |
| DAC Resolution | | (Note1) | -- | 8 | -- | bits |
| DAC Differential Nonlinearity | | (Note1) | -- | -- | 0.5 | LSB |
| **Power Good** | | | | | | |
| Power Good Threshold | $V_{TH\_PGLH}$ | $V_{OUT}$ rising, PGOOD from low to high | -- | 87 | -- | % of $V_{REF}$ |
| | $V_{TH\_PGHL}$ | $V_{OUT}$ falling, PGOOD from high to low | -- | 77 | -- | |
| Power Good Falling Delay Time | | | -- | 3 | -- | µs |

(1) Note 1 for $\theta_{JA(EVB)}$, $\Psi_{JC(Top)}$ and $\Psi_{JB}$ are measured on a high effective-thermal-conductivity four-layer test board which is in size of 70mm x 50mm, furthermore, all layers with 1 oz. Thermal resistance/parameter values may vary depending on the PCB material, layout, and test environmental conditions.

(2) Note 2 for guaranteed by design

*Table 4-3. $I^2C$ Interface (The $I^2C$ interface will not work until the RESET# goes high)*

| Parameter | Symbol | Test Conditions | Min | Typ | Max | Unit |
|---|---|---|---|---|---|---|
| SDA, SCL Input Voltage | High Level | | 1.2 | -- | -- | V |
| | Low Level | | -- | -- | 0.4 | V |
| SCL Clock Rate | $f_{SCL}$ | Fast mode | -- | -- | 400 | kHz |
| | | Fast mode plus | -- | -- | 1 | MHz |
| | | High speed mode, load 100pF max | -- | -- | 3.4 | MHz |
| Hold Time (Repeated) Start Condition. After this Period, the First Clock Pulse is Generated | $t_{HD;STA}$ | Fast mode | 0.6 | -- | -- | µs |
| | | Fast mode plus | 0.26 | -- | -- | µs |
| | | High speed mode | 0.16 | | | µs |
| Low Period of the SCL Clock | $t_{LOW}$ | Fast mode | 1.3 | -- | -- | µs |
| | | Fast mode plus | 0.5 | -- | -- | µs |
| | | High speed mode | 0.16 | | | µs |
| High Period of the SCL Clock | $t_{HIGH}$ | Fast mode | 0.6 | -- | -- | µs |
| | | Fast mode plus | 0.26 | -- | -- | µs |
| | | High speed mode | 0.06 | | | µs |
| Set-Up Time for a Repeated START Condition | $t_{SU;STA}$ | Fast mode | 0.6 | -- | -- | µs |
| | | Fast mode plus | 0.26 | -- | -- | µs |
| | | High speed mode | 0.01 | | | µs |
| Data Hold Time | $t_{HD;DAT}$ | Fast mode | 0 | -- | -- | µs |
| | | Fast mode plus | 0 | -- | -- | µs |
| | | High speed mode | 0 | -- | -- | µs |
| Data Set-Up Time | $t_{SU;DAT}$ | Fast mode | 100 | -- | -- | ns |
| | | Fast mode plus | 50 | -- | -- | ns |
| | | High speed mode | 10 | -- | -- | ns |
| Set-Up Time for STOP Condition | $t_{SU;STO}$ | Fast mode | 0.6 | -- | -- | µs |
| | | Fast mode plus | 0.26 | -- | -- | µs |
| | | High speed mode | 0.16 | -- | -- | µs |
| Bus Free Time between a STOP and START Condition | $t_{BUF}$ | Fast mode | 1.3 | -- | -- | µs |
| | | Fast mode plus | 0.5 | -- | -- | µs |
| Rising Time of both SDA and SCL Signals | $t_R$ | Fast mode | 20 | -- | 300 | ns |
| | | Fast mode plus | -- | -- | 120 | ns |
| | | High speed mode (SDA) load 100pF max | 10 | -- | 80 | ns |
| | | High speed mode (SCL) load 100pF max | 10 | -- | 40 | ns |

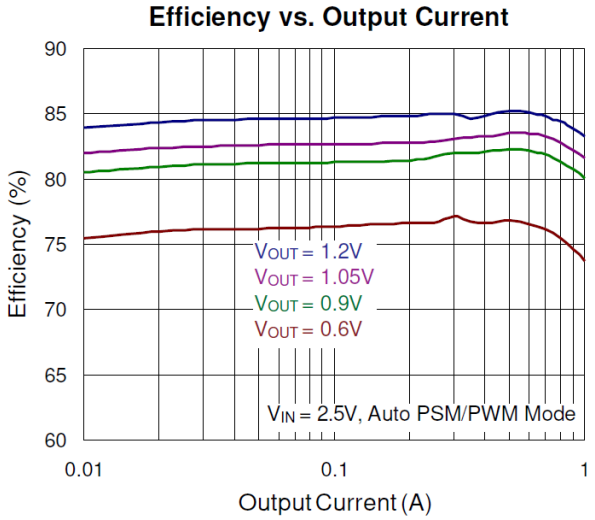
**Note:**

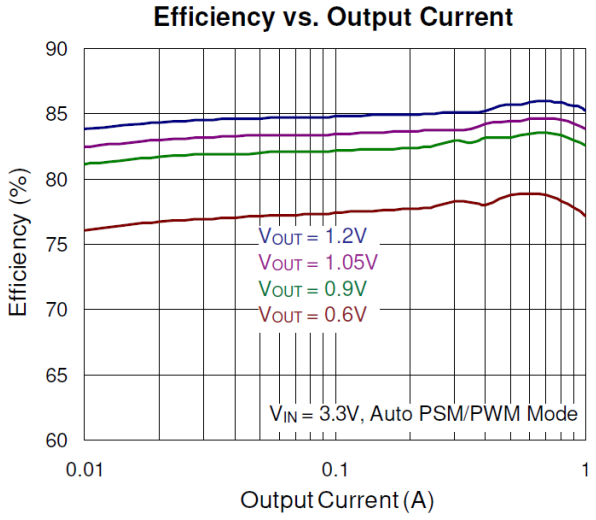
Guaranteed by design.

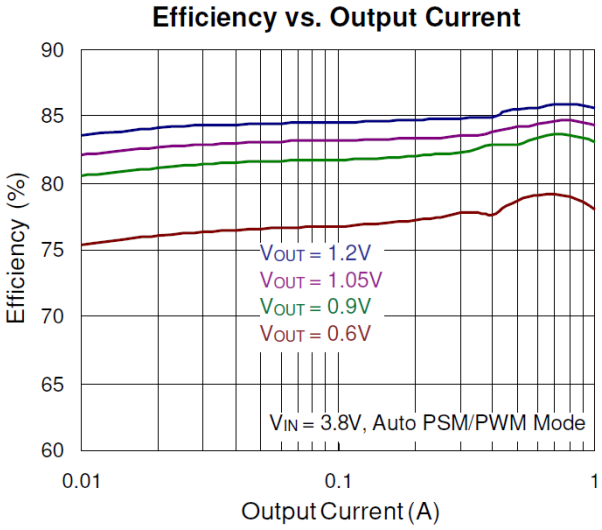
# 5 Typical Operating Characteristics

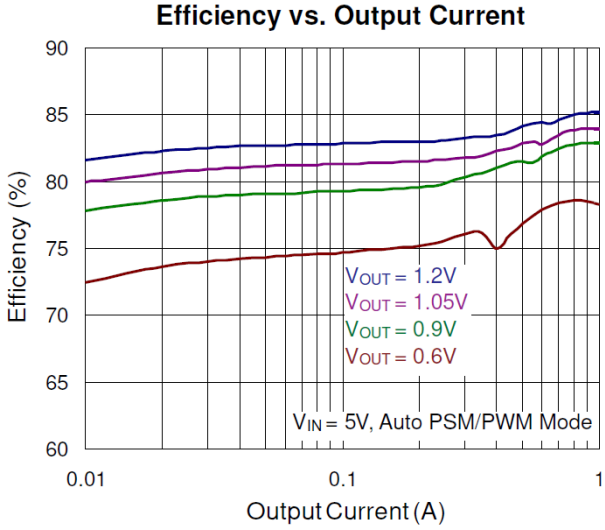
## 5.1 Typical Operating Characteristics

Unless otherwise specified, Auto PFM/PWM mode, $T_A$ = 25°C; circuit and components according to typical application circuit and Table 6-10.

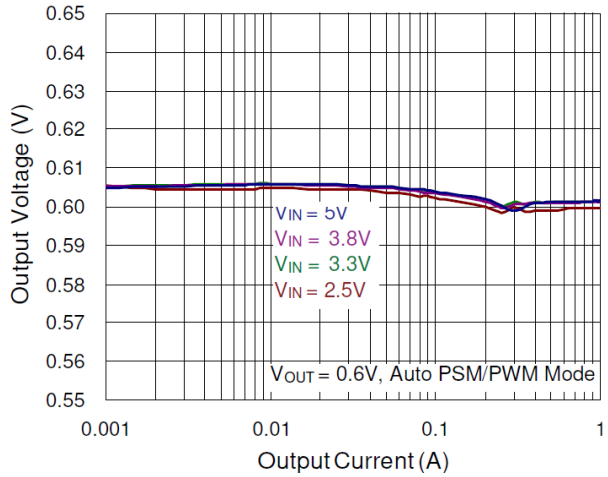


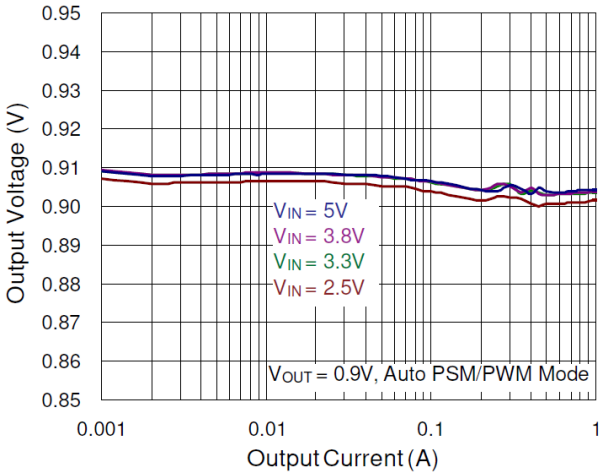



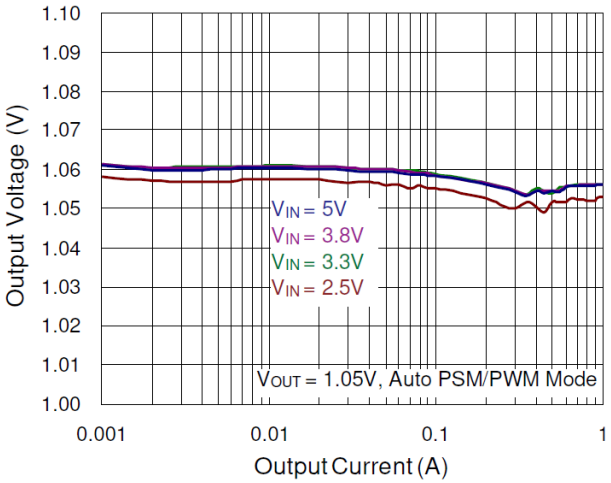
**Output Voltage vs. Output Current**



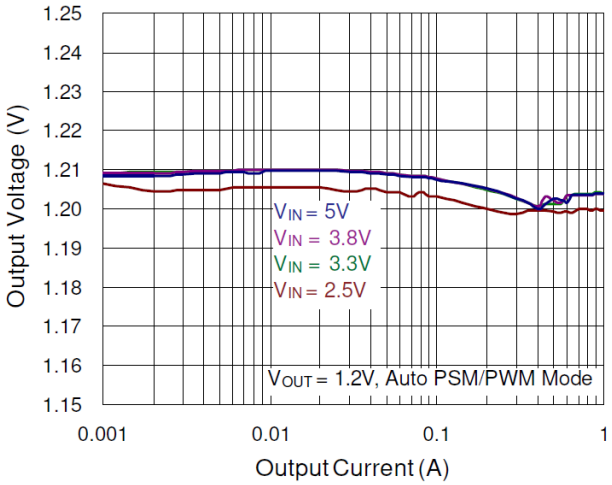

**Output Voltage vs. Output Current**



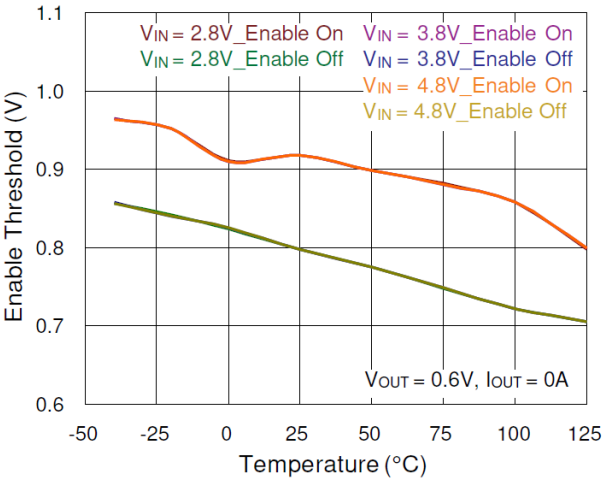

**Output Voltage vs. Output Current**



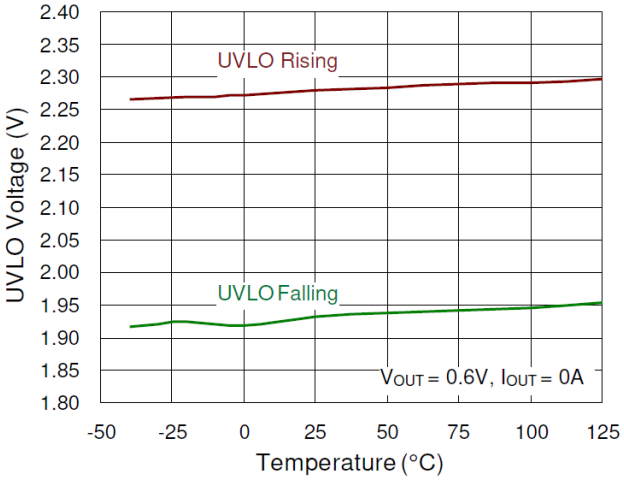

**Output Voltage vs. Output Current**



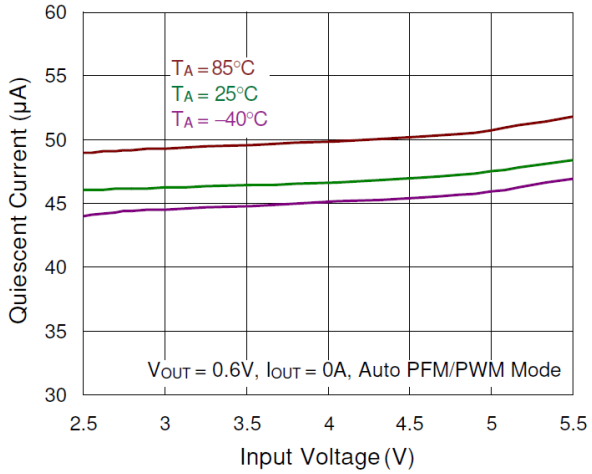

**Enable Threshold vs. Temperature**



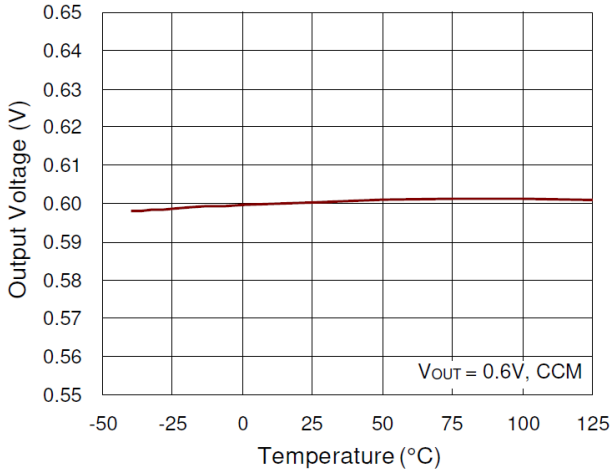

**UVLO Voltage vs. Temperature**



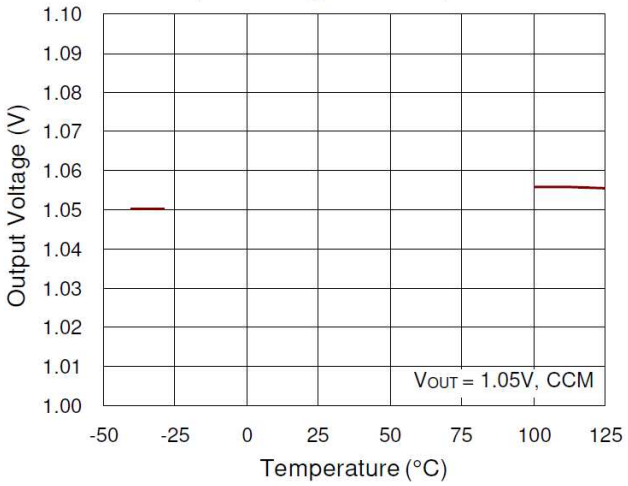
**Quiescent Current vs. Input Voltage**



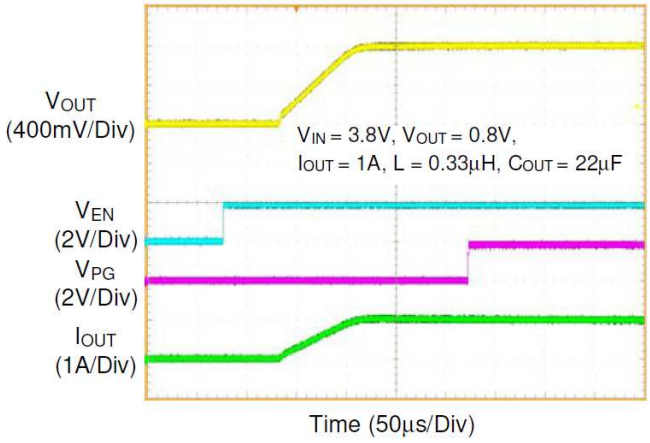

**Output Voltage vs. Temperature**



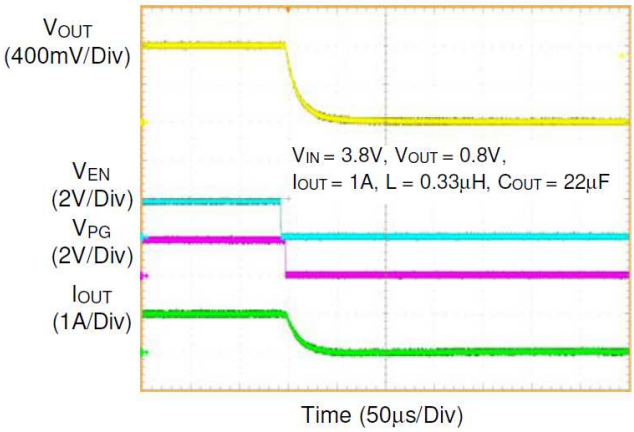

**Output Voltage vs. Temperature**



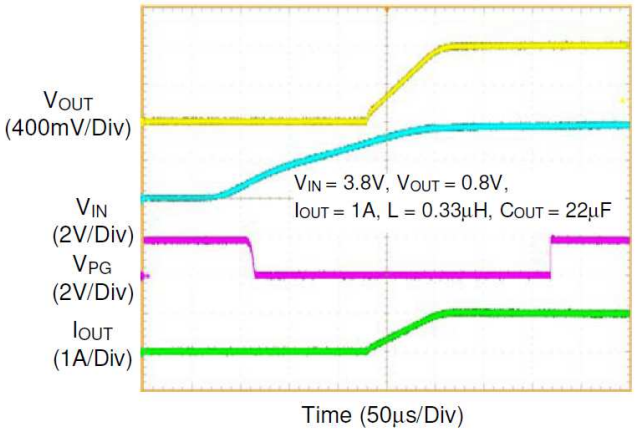

**Power On from EN**



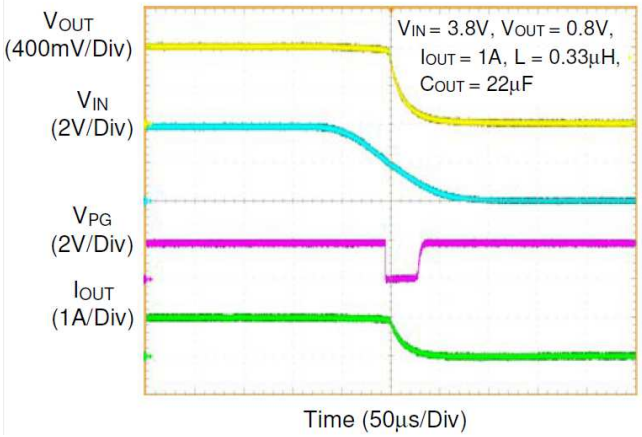

**Power Off from EN**



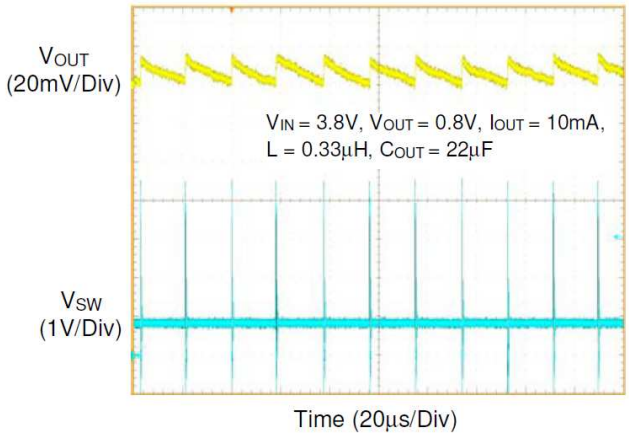

**Power On from VIN**



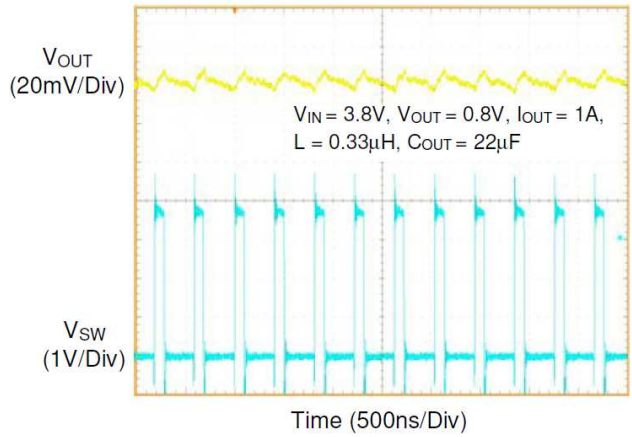
**Power Off from VIN**



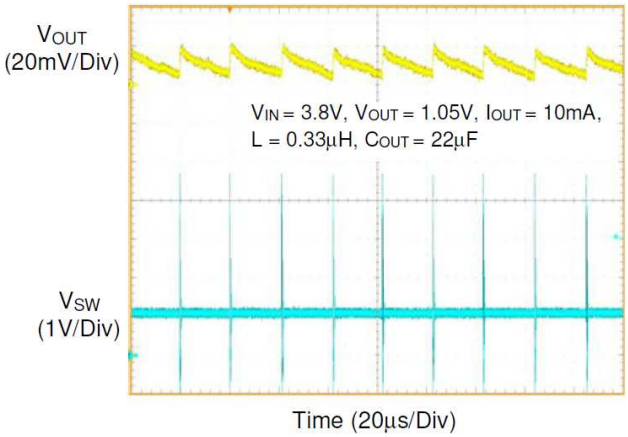

**Output Ripple as $I_{OUT}$ = 10mA**



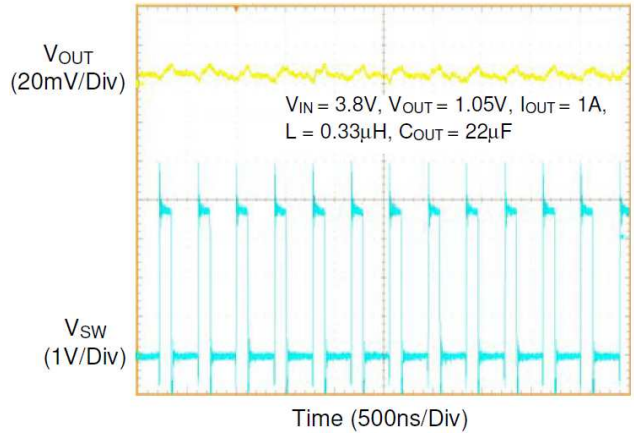

**Output Ripple as $I_{OUT}$ = 1A**



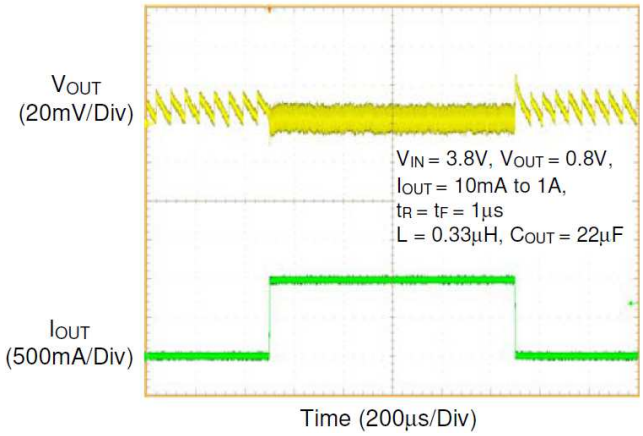

**Output Ripple as $I_{OUT}$ = 10mA**



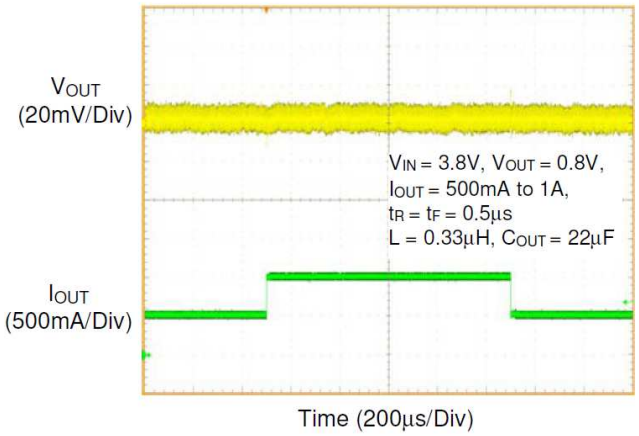

**Output Ripple as $I_{OUT}$ = 1A**



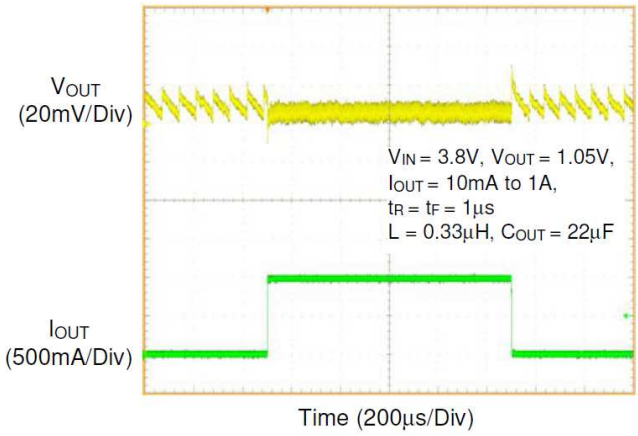

**Load Transient Response**



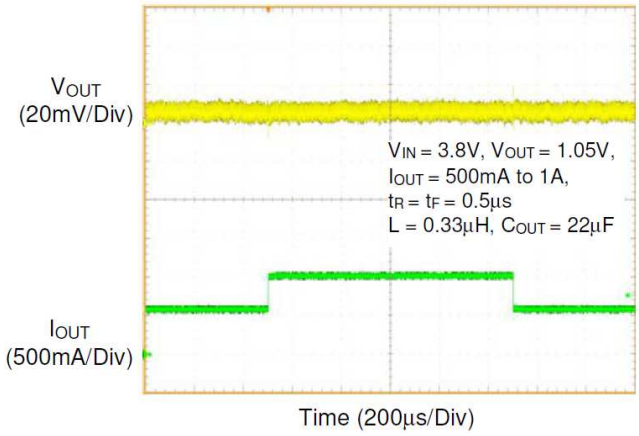
### Load Transient Response



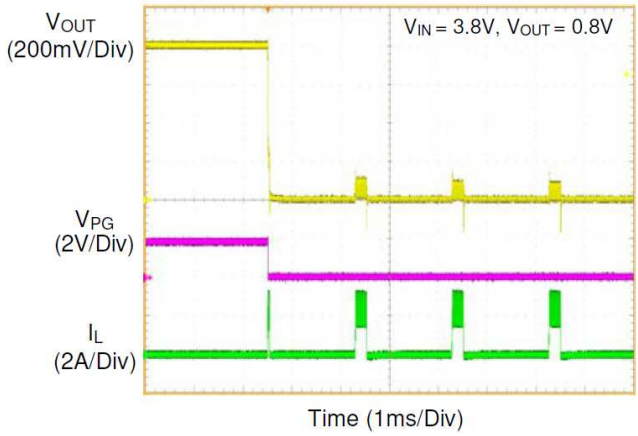

### Load Transient Response



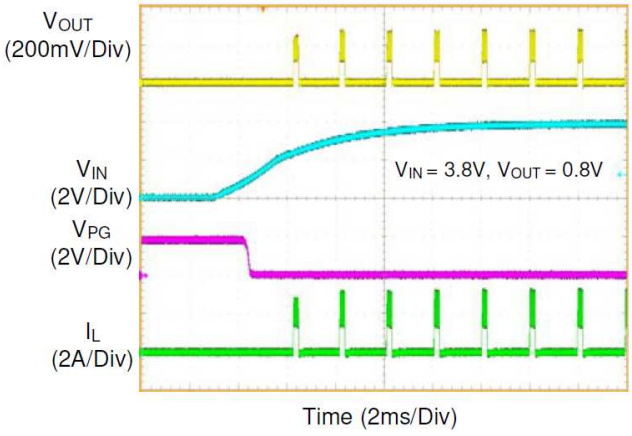

### Load Transient Response




### Over-Current Protection




### Short-Circuit before Power On



# 6 Application Information

The basic MA5721 application circuit is shown in Typical Application Circuit. External component selection is determined by the maximum load current and begins with the selection of the inductor value and operating frequency followed by $C_{IN}$ and $C_{OUT}$.

## 6.1 Inductor Selection

The inductor value and operating frequency determine the ripple current according to a specific input and output voltage. The ripple current, $\otimes I_L$, increases with higher $V_{IN}$ and decreases with higher inductance, as shown in the equation below :

$$\Delta I_L = \left[\frac{V_{OUT}}{f \times L}\right] \times \left[1 - \frac{V_{OUT}}{V_{IN}}\right]$$

where f is the operating frequency and L is the inductance. To optimize the loop stability, 0.33µH is strongly recommended. Suppose the higher inductance is chosen, the transient performance may become worse; in the opposite situation, the lower inductance causes larger ripple, and there is a risk of reaching negative over-current protection during VID down.

## 6.2 Input and Output Capacitor Selection

An input capacitor, $C_{IN}$, is needed to filter out the trapezoidal current at the source of the high-side MOSFET.
To prevent large ripple current, a low ESR input capacitor sized for the maximum RMS current should be used. The RMS current is given by :

$$I_{RMS} = I_{OUT(MAX)} \times \frac{V_{OUT}}{V_{IN}} \times \sqrt{\frac{V_{IN}}{V_{OUT}} - 1}$$

This formula has a maximum at $V_{IN} = 2V_{OUT}$, where $I_{RMS} = I_{OUT(MAX)} / 2$.
This simple worst-case condition is commonly used for design.
Choose a capacitor rated at a higher temperature than required.
Several capacitors may also be paralleled to meet the size or height requirements of the design. Ceramic capacitors have high ripple current, high voltage rating and low ESR, which makes them ideal for switching regulator applications. However, they can also have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can lead to significant ringing. When a ceramic capacitor is used at the input and the power is supplied by a wall adapter through long wires, a load step at the output can induce ringing at the input, $V_{IN}$. At best, this ringing can couple to the output and be mistaken as loop instability. At worst, a sudden inrush of current through the long wires can potentially cause a voltage spike at $V_{IN}$ large enough to damage the part. Thus, care must be taken to select a suitable input capacitor.
The selection of $C_{OUT}$ is determined by the required ESR to minimize output voltage ripple. Moreover, the amount of bulk capacitance is also a key for $C_{OUT}$ selection to ensure that the control loop is stable. Loop stability can be checked by viewing the load transient response.
The output voltage ripple, $\otimes V_{OUT}$, is determined by :

$$\Delta V_{OUT} \leq \Delta I_L \left[ESR + \frac{1}{8 \times f_{SW} \times C_{OUT}}\right]$$

where $f_{SW}$ is the switching frequency and $\otimes I_L$ is the inductor ripple current. The output voltage ripple will be the highest at the maximum input voltage since $\otimes I_L$ increases with input voltage. Multiple capacitors placed in parallel may be needed to

meet the ESR and RMS current handling requirement.

Ceramic capacitors have excellent low ESR characteristics, but can have a high voltage coefficient and audible piezoelectric effects. The high Q of ceramic capacitors with trace inductance can also lead to significant ringing.

Nevertheless, high value, low-cost ceramic capacitors are now becoming available in smaller case sizes. Their high ripple current, high voltage rating and low ESR make them ideal for switching regulator applications.

## 6.3 I²C Interface Function

The MA5721 can be managed by I²C interface to select $V_{OUT}$ voltage level, Dynamic Voltage Scaling (DVS) slew rate, Auto PFM/PSM or Forced PWM mode, and so on.

The register of each function can be found from the following register map, which also explains how to use these functions.

The MA5721 all series IC are able to support fast mode I²C interface (bit rate 400kb/s). For example, the MA5721A default I²C slave address is 7'b1010000. The write or read bit stream (N ≥ 1) is shown below :

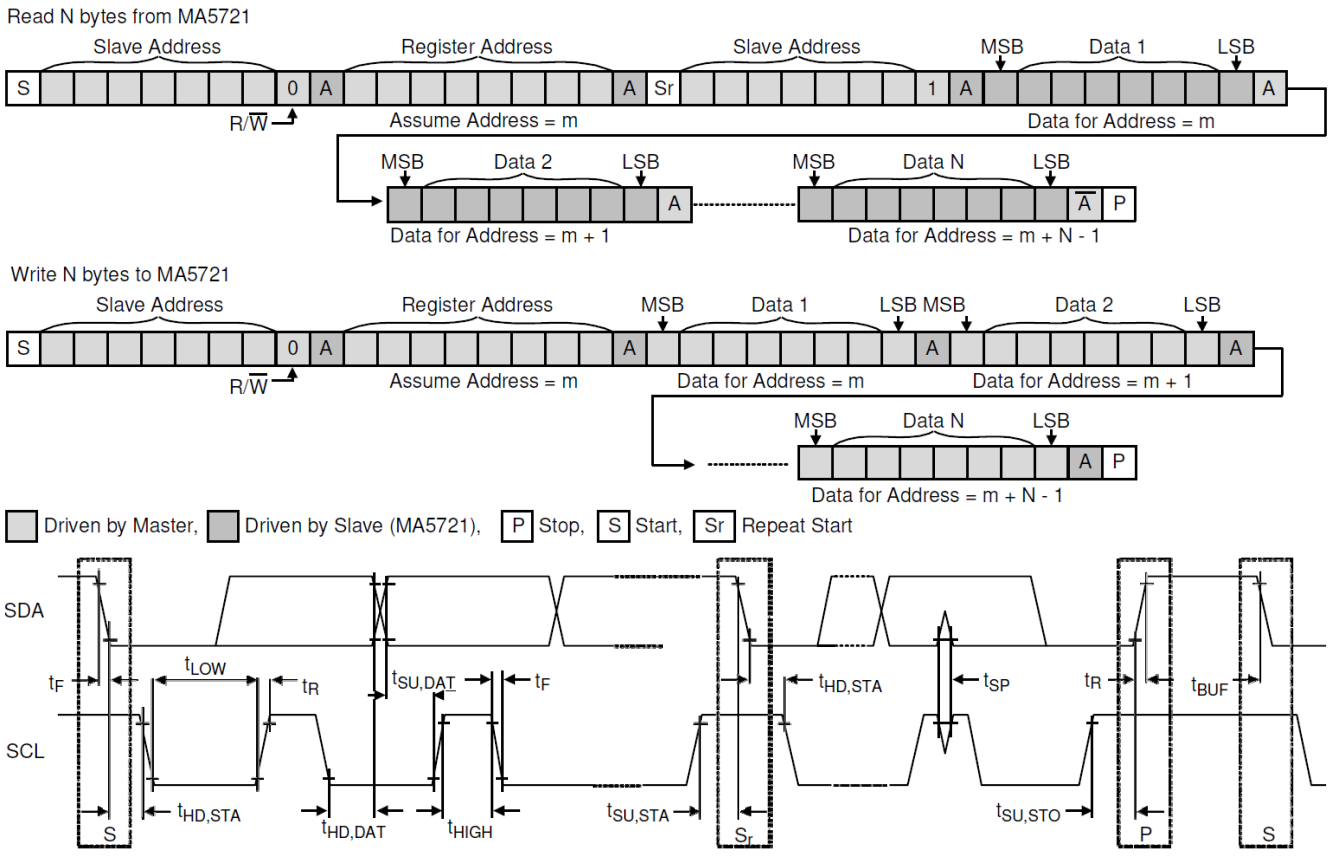



***Figure 6-1. I²C Read and Write Stream and Timing Diagram***

The MA5721 also supports High-speed mode (bit rate up to 3.4Mb/s) with access code 08H. Figure 6-2 and Figure 6-3 show detailed transfer format. Hs-mode can only commence after the following conditions (all of which are in F/S-mode) :

- START condition (S)
- 8-bit master code (00001xxx)
- not-acknowledge bit (Ā)

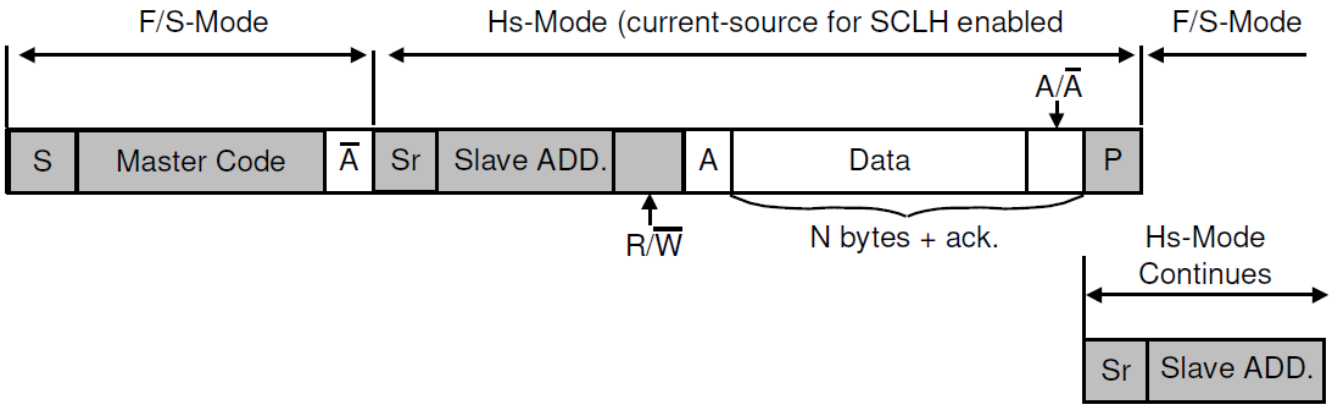



*Figure 6-2. Data Transfer Format in Hs-mode*

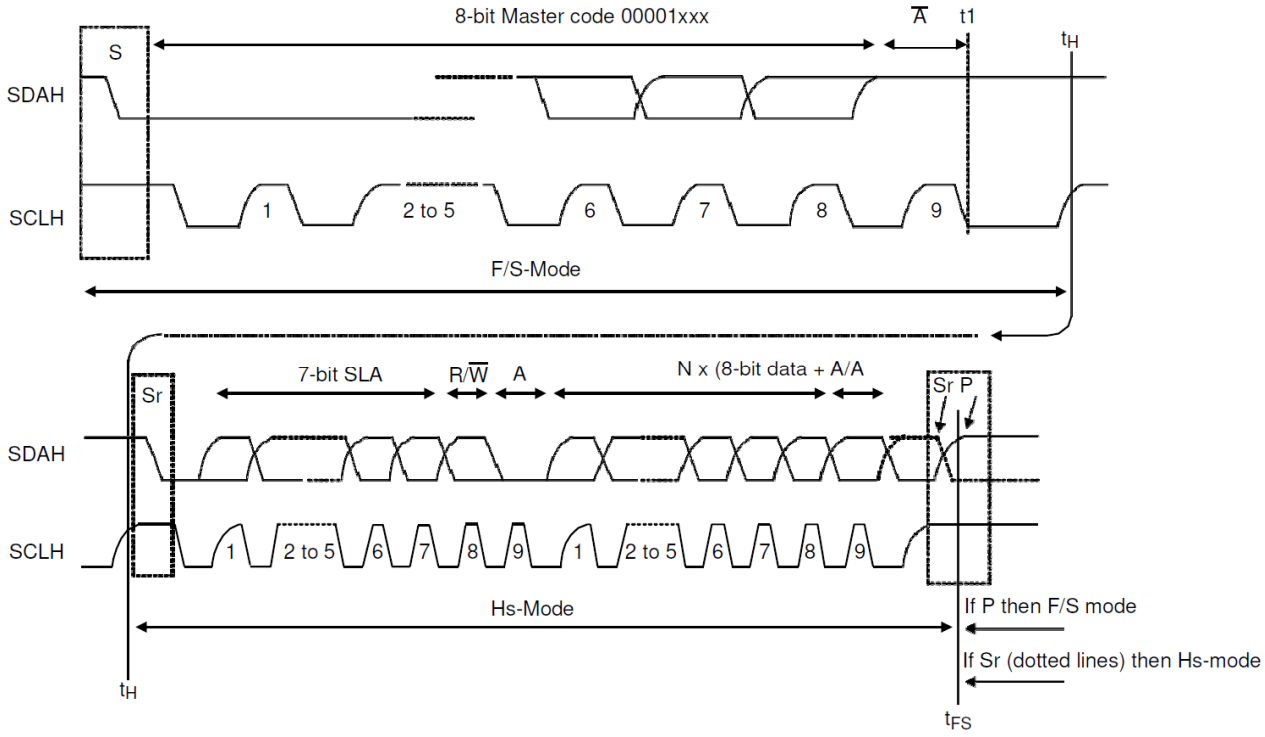



*Figure 6-3. A Complete Hs-mode Transfer*

- The MA5721A I²C slave address is 7'b1010100 for 0.9V/0.8V setting.
- The MA5721B I²C slave address is 7'b1010101 for 0.9V/1.05V setting.
- The MA5721C I²C slave address is 7'b1010110 for 0.6V/0.4V setting.
- The MA5721D I²C slave address is 7'b1010111 for 1.125V/1.125V setting.
- The MA5721E I²C slave address is 7'1010100 for 0.8V/0.75V setting.
- The MA5721F I²C slave address is 7'b1010101 for 0.75V/0.75V setting.

*Table 6-1. I²C Register Map*

| Register Name | Address | Bit 7 | Bit 6 | Bit 5 | Bit 4 | Bit 3 | Bit 2 | Bit 1 | Bit 0 | Type |
|---|---|---|---|---|---|---|---|---|---|---|
| NSEL0 | 0x00 | VSEL0 | | | | | | | | RW |
| NSEL1 | 0x01 | VSEL1 | | | | | | | | RW |
| CONTROL1 | 0x02 | DISCHG | UP_SR[2:0] | | | Reserved | SW_RESET | MODE_VSEL1 | MODE_VSEL0 | R/W |
| ID1 | 0x03 | VENDOR_ID | | | Reserved | DIE_ID | | | | R |
| ID2 | 0x04 | Reserved | | | | DIE_REV | | | | R |
| MONITOR | 0x05 | PGOOD | UVLO | Reserved | POS | NEG | RESET_STAT | OT | BUCK_STATUS | R |
| CONTROL2 | 0x06 | DN_SR[2:0] | | | Reserved | SS_SR[1:0] | | EN_VSEL1 | EN_VSEL0 | R/W |
| CONTROL4 | 0x08 | Reserved | | DIS_DLY[5:0] | | | | | | R/W |

*Table 6-2. NSEL0*

| Address: 0x00 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | VSEL0 | | | | | | | |
| MA5721A | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| MA5721B | 0 | 1 | 1 | 1 | 1 | 0 | 0 | 0 |
| MA5721C | 0 | 0 | 1 | 1 | 1 | 1 | 0 | 0 |
| MA5721E | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| MA5721D | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| MA5721F | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | VSEL0 | VID Table satisfy:<br>SEL[7:0] = 11001000: $V_{OUT}$ = 1.3V<br>...<br>SEL[7:0] = 00000000: 0.3V<br>5mV step for 0.3V to 1.3V |

*Table 6-3. NSEL1*

| Address: 0x01 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | VSEL1 | | | | | | | |
| MA5721A | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| MA5721B | 1 | 0 | 0 | 1 | 0 | 1 | 1 | 0 |
| MA5721C | 0 | 0 | 0 | 1 | 0 | 1 | 0 | 0 |
| MA5721E | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| MA5721D | 1 | 0 | 1 | 0 | 0 | 1 | 0 | 1 |
| MA5721F | 0 | 1 | 0 | 1 | 1 | 0 | 1 | 0 |
| MA5721A | 0 | 1 | 1 | 0 | 0 | 1 | 0 | 0 |
| Type | RW | | | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:0 | VSEL1 | VID Table satisfy:<br>SEL[7:0] = 1100100 0: $V_{OUT}$ = 1.3V<br>...<br>SEL[7:0] = 00000000: 0.3V<br>5mV step for 0.3V to 1.3V |

*Table 6-4. DISCHG*

| Address: 0x02 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | DISCHG | UP_SR | | | Reserved | SW_RESET | MODE_VSEL1 | MODE_VSEL0 |
| MA5721F | 1 | 0 | 0 | 1 | 0 | 0 | 1 | 0 |
| Others | 1 | 0 | 0 | 1 | 0 | 0 | 0 | 0 |
| Type | RW | RW | | | RV | RW | RW | RW |

| Bit | Name | Description |
|---|---|---|
| 7 | DISCHG | 0: Discharge path disabled<br>1: Discharge path enabled |
| 6:4 | UP_SR | DVS Speed for UP DVS<br>000 = 24mV/µs<br>001 = 12mV/µs<br>010 = 6mV/µs<br>011 = 3mV/µs<br>100 = 1.5mV/µs<br>101 = 0.75mV/µs<br>110 = 0.375mV/µs<br>111 = 0.1875mV/µs |
| 3 | Reserved | Reserved bits |
| 2 | SW_RESET | Write 1 to reset, always read 0 |
| 1 | MODE_VSEL1 | Mode control (activate when the VSEL pin set to logic-high):<br>1: Forced PWM mode<br>0: Auto PFM/PWM mode |
| 0 | MODE_VSEL0 | Mode control (activate when the VSEL pin set to logic-low):<br>1: Forced PWM mode<br>0: Auto PFM/PWM mode |

*Table 6-5. ID1*

| Address: 0x03 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | VENDOR_ID | | | Reserved | DIE_ID | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RO | | | RV | RO | | | |

| Bit | Name | Description |
|---|---|---|
| 7:5 | VENDOR_ID | Vendor_ID |
| 4 | Reserved | Reserved bits |
| 3:0 | DIE_ID | DIE_ID |

*Table 6-6. ID2*

| Address: 0x04 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | | | DIE_REV | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RV | | | | RO | | | |

| Bit | Name | Description |
|---|---|---|
| 7:4 | Reserved | Reserved bits |
| 3:0 | DIE_REV | Revision_ID |

*Table 6-7. MONITOR*

| Address: 0x05 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | PGOOD | UVLO | Reserved | POS | NEG | RESET_STAT | OT | BUCK_STATUS |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RO | RO | RV | RO | RO | RO | RO | RO |

| Bit | Name | Description |
|---|---|---|
| 7 | PGOOD | 1: Buck is enabled and soft-start is completed. |
| 6 | UVLO | 1: Signifies the VIN is less than the UVLO threshold. |
| 5 | Reserved | Reserved bits |
| 4 | POS | 1: Signifies a positive voltage transition is in progress |
| 3 | NEG | 1: Signifies a negative voltage transition is in progress |
| 2 | RESET_STAT | 1: Indicates that a register reset was performed. |
| 1 | OT | 1: Signifies the thermal shutdown is active. |
| 0 | BUCK_STATUS | 1: Buck enabled; 0: buck disabled. |

*Table 6-8. CONTROL2*

| Address: 0x06 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | DN_SR | | | Reserved | SS_SR | | EN_VSEL1 | EN_VSEL0 |
| Default | 0 | 1 | 1 | 0 | 0 | 0 | 1 | 1 |
| Type | RW | | | RV | RW | | RW | RW |

| Bit | Name | Description |
|---|---|---|
| 7:5 | DN_SR | DVS Speed for DN DVS<br>000 = 24 mV/µs<br>001 = 12 mV/µs<br>010 = 6 mV/µs<br>011 = 3 mV/µs<br>100 = 1.5 mV/µs<br>101 = 0.75 mV/µs<br>110 = 0.375 mV/µs<br>111 = 0.1875 mV/µs |
| 4 | Reserved | Reserved bits |
| 3:2 | SS_SR | DVS Speed for soft start DVS<br>00 = 10mV/µs<br>01 = 5mV/µs<br>10 = 2.5mV/µs<br>11 = 1.25mV/µs |
| 1 | EN_VSEL1 | Software power-on/off control register (activate when the VSEL pin set to logic-high):<br>0: Disable output<br>1: Enable output |
| 0 | EN_VSEL0 | Software power-on/off control register (activate when the VSEL pin set to logic-low):<br>0: Disable output<br>1: Enable output |

*Table 6-9. CONTROL4*

| Address: 0x08 | | | | | | | | |
|---|---|---|---|---|---|---|---|---|
| Bit | 7 | 6 | 5 | 4 | 3 | 2 | 1 | 0 |
| Field | Reserved | | DIS_DLY | | | | | |
| Default | 0 | 0 | 0 | 0 | 0 | 0 | 0 | 0 |
| Type | RV | | RW | | | | | |

| Bit | Name | Description |
|---|---|---|
| 7:6 | Reserved | Reserved bits |
| 5:0 | DIS_DLY | Delay applied upon disable (ms)<br>000000b = 0ms - 111111b = 63ms(steps of 1ms) |

## 6.4 $V_{OUT}$ Selection

The MA5721 has programmable $V_{OUT}$ from 0.3V to 1300mV with 5mV resolution.
The output voltage can be set by NSELx register bit and the output voltage is given by the following equation :
$V_{OUT}$ = 0.3V + NSELx x 5mV
For example :
if NSELx = 0111100 (60 decimal), then $V_{OUT}$ = 0.3 + 60 x 5mV = 0.3 + 0.3 = 0.6V.
The MA5721 also has external VSEL pin to select NSEL1(0X01) or NSEL0(0X00). Pulling VSEL to high is for VSEL1 and pulling VSEL to low is for VSEL0.
Upon POR, VSEL0 and VSEL1 are reset to their default voltages.

## 6.5 Enable and Soft-Start

When the EN pin is LOW, the IC is shut down, all internal circuits are off, and the part draws very little current. In this state, $I^2C$ cannot be written to or read until enable voltage is above the enable rising threshold. The registers are reset when the EN pin is LOW or during a Power On Reset (POR).
Once the EN pin is high, $V_{OUT}$ will ramp up at the chosen soft-start slew rate programmed in the CONTROL2 register SS_SR bit.

## 6.6 Discharge Function

In the CONTROL1 register, setting the DISCHG bit to 1 can make $V_{OUT}$ discharge by internal resistor when the converter shuts down. If the DISCHG bit is set to 0, $V_{OUT}$ will decrease depending on the loading. When EN pin is set to low, the MA5721 turns on 10∧ discharge resistor by default.

## 6.7 Slew Rate Setting

The MA5721 can control slew rate as $V_{OUT}$ changes between two voltage levels for both up and down.
The UP_SR bits in the CONTROL1 register control up- speed, whereas the DN_SR bits in the CONTROL2 register control down-speed. The default DVS up slew rate is 12mV/µs and DVS down slew rate is 3mV/µs.

## 6.8 Forced PWM Mode

The MODE_VSEL0 and MODE_VSEL1 bits in CONTROL1 register can determine the operation mode of the converter. Set 1 for Forced PWM operation and set 0 for auto PSM/ PWM operation. Note that, MODE_VSEL0 is activated only when pulling VSEL pin to low, and only set VSEL pin to high for VSEL1 so that the setting of MODE_VSEL1 can be activated.
During dynamic voltage scaling from high setting of output voltage to low setting, the MA5721 makes transient in Forced PWM mode, and output voltage will decrease quickly.

## 6.9 Typical Application Circuit

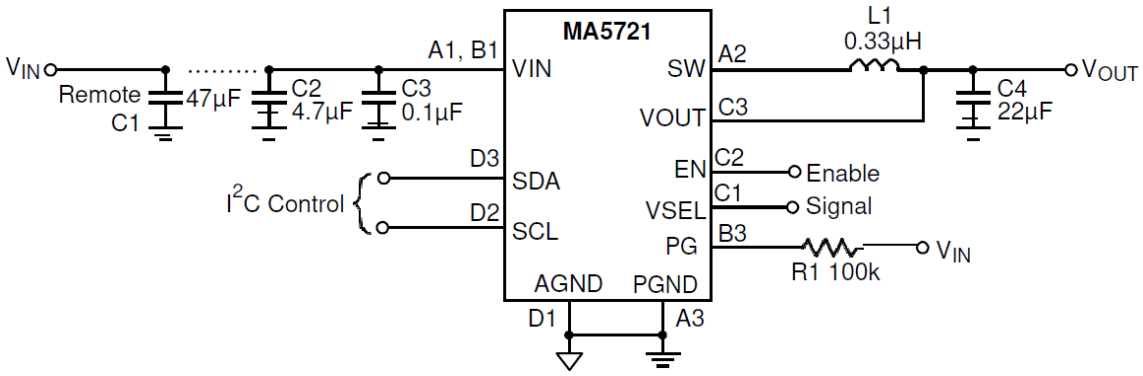



***Figure 6-4. Typical application circuit***

***Table 6-10. Recommended External Components for 1A Maximum Load Current***

| Component | Description | Vendor P/N |
|---|---|---|
| L1 | 330nH, 2016 case size | DFE201610E-R33M=P2 (Murata) |
| | | HMMQ20161T-33MDR (Cyntec) |
| C2 | 4.7µF, 10V, X5R, 0402 | ZRB15XR61A475ME01D (Murata) |
| C3(1) | 100nF, 6.3V, X5R, 0201 | GRM033R60J104KE19D (Murata) |
| C4 | 22µF, 6.3V, X5R, 0603 | GRM188R60J226MEA0D (Murata) |
| | | C1608X5R0J226M080AC (TDK) |

(1) Note 1 for the decoupling capacitor C3 is recommended to reduce any high frequency component on VIN bus. All the input and output capacitors are the suggested values, referring to the effective capacitances, subject to any de-rating effect, like a DC bias.

## 6.10 Thermal Considerations

The junction temperature should never exceed the absolute maximum junction temperature $T_{J(MAX)}$, listed under Absolute Maximum Ratings, to avoid permanent damage to the device. The maximum allowable power dissipation depends on the thermal resistance of the IC package, the PCB layout, the rate of surrounding airflow, and the difference between the junction and ambient temperatures. The maximum power dissipation can be calculated using the following formula :

$$P_{D(MAX)} = (T_{J(MAX)} - T_A) / \theta_{JA}$$

where $T_{J(MAX)}$ is the maximum junction temperature, $T_A$ is the ambient temperature, and $\theta_{JA}$ is the junction-to-ambient thermal resistance.

For continuous operation, the maximum operating junction temperature indicated under Recommended Operating Conditions is 125°C. The junction-to-ambient thermal resistance, $\theta_{JA}$, is highly package dependent. For a WL-CSP-11B 1.31x1.62 (BSC) package, the thermal resistance, $\theta_{JA}$, is 68.5°C/W on a standard JEDEC 51-7 high effective-thermal-conductivity four-layer test board.

The maximum power dissipation at $T_A$ = 25°C can be calculated as below :
$P_{D(MAX)}$ = (125°C - 25°C) / (68.5°C/W) = 1.46W for a WL-CSP-11B 1.31x1.62 (BSC) package.

The maximum power dissipation depends on the operating ambient temperature for the fixed $T_{J(MAX)}$ and the thermal resistance, $\theta_{JA}$. The derating curves in Figure 6-5 allows the designer to see the effect of rising ambient temperature on the maximum power dissipation.

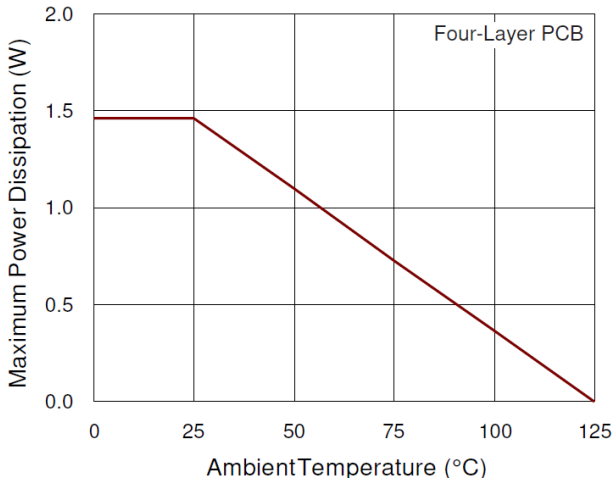



***Figure 6-5. Derating Curve of Maximum Power Dissipation***

## 6.11 Layout Considerations

For best performance of the MA5721, the following layout guidelines must be strictly followed.

- Input capacitor must be placed as close as possible to IC to minimize the power loop area. A typical 0.1µF decoupling capacitor is recommended to reduce power loop area and any high frequency component on $V_{IN}$.
- SW node is with high frequency voltage swing, so the SW node area should be kept small.
- Keep every power trace connected to pin as wide as possible for improving thermal dissipation.
- The AGND pin is suggested to connect to 2nd GND plate through top to 2nd via.

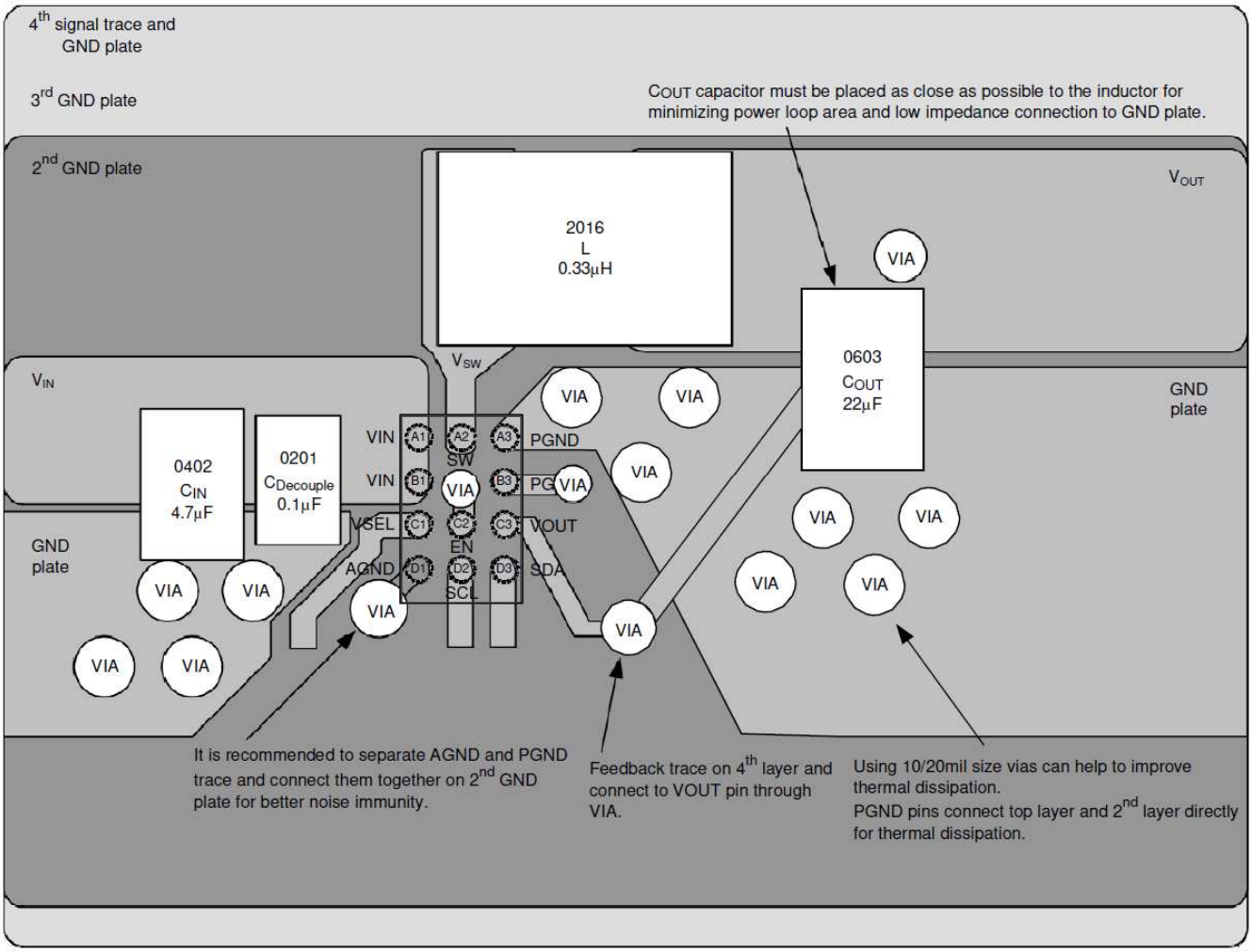
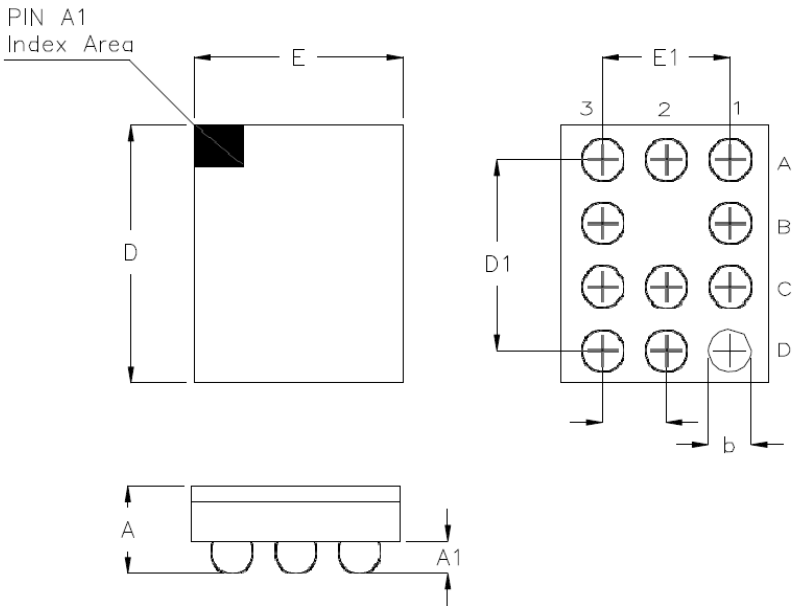



***Figure 6-6. PCB Layout Guide***

# 7 MA5721 Packaging

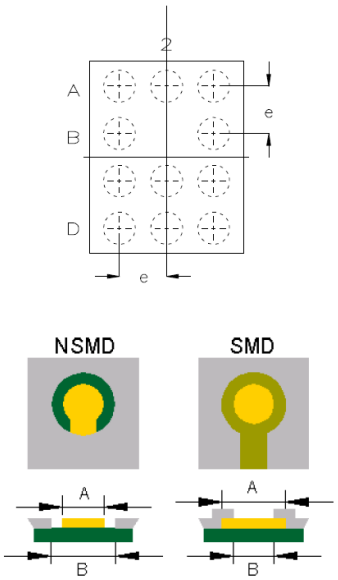
## 7.1 Outline Dimension




| Symbol | Dimensions In Millimeters | | Dimensions In Inches | |
|---|---|---|---|---|
| | Min | Max | Min. | Max |
| A | 0.500 | 0.600 | 0.020 | 0.024 |
| A1 | 0.170 | 0.230 | 0.007 | 0.009 |
| b | 0.240 | 0.300 | 0.009 | 0.012 |
| D | 1.580 | 1.660 | 0.062 | 0.065 |
| D1 | 1.200 | | 0.047 | |
| E | 1.270 | 1.350 | 0.050 | 0.053 |
| E1 | 0.800 | | 0.031 | |
| e | 0.400 | | 0.016 | |

***Figure 7-1. 11B WL-CSP 1.31x1.62 Package (BSC)***

## 7.2 Footprint Information




| Package | Number of Pin | Type | Footprint Dimension (mm) | | | Tolerance |
|---|---|---|---|---|---|---|
| | | | e | A | B | |
| WL-CSP1.31x1.62-11(BSC) | 11 | NSMD | 0.400 | 0.240 | 0.340 | ±0.025 |
| | | SMD | | 0.270 | 0.240 | |

***Figure 7-2. Footprint information***

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