MT7933CT Datasheet
802.11a/b/g/n/ac/ax Wi-Fi 1T1R
+ Bluetooth 5.2 + ARM® Cortex®-M33

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Version History

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0.1	2021-05-30	MediaTek	Initial draft
0.92	2021-07-15	MediaTek	Revised version
0.93	2021-08-30	MediaTek	1. Correct Audio Codec
0.94	2021-11-14	MediaTek	1. Update the PinMux table, RF performance, LP data, power-on sequence and top marking
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1.1	2022-11-25	MediaTek	1. All content is same as v1.0, only update MediaTek document secure label

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0 Features

Wi-Fi

- IEEE 802.11 1T1R a/b/g/n/ac/ax 5 GHz and 2.4 GHz bands
- Supports 1x1 20 MHz bandwidth, MCS0~8(256-QAM) in 2.4/5 GHz band
- Support MU-MIMO RX
- Support uplink MU-OFDMA TX and downlink MU-OFDMA RX
- Support Tx LDPC(Low-density parity check)
- Support Rx Beamformee
- Support RX STBC
- Wi-Fi security WFA WPA/WPA2/WPA3 personal
- QoS support of WFA WMM
- Integrated balun, PA, LNA, and T/R switch
- Support CSI (Channel Signal Information)
- Supports antenna diversity
- Optional external LNA and PA support

Bluetooth

- BT5.2 LE Isochronous Channel
- BT5.1 Advertising Enhancement
- BT5.0 2M_PHY / Long Range / Advertising Extension / SAM / CS#2 / High Duty Cycle Non-Connectable ADV
- BT4.2 Link Layer Privacy / LE Secure Connection / LE Data Packet Length Extension / Link Layer Extended Scanner Filter Policies
- BT4.1 Link Layer Topology / Secure Connection
- BT4.0 and below BR/EDR
- BR/EDR and BLE dual mode concurrent
- Integrated balun and PA
- Scatternet support: Up to 7 piconets simultaneously with background inquiry/page scan
- Up to 4 BT links + 8 BLE links
- Support SCO and eSCO link with re-transmission
- Packet loss concealment
- Channel quality driven data rate adaptation
- Channel assessment and WB RSSI for AFH

Microcontroller Subsystem

- ARM® Cortex®-M33 with floating point unit (FPU) with 300-MHz clock rate
- Supports 12 DMA channels
- Embedded 8MB UHS SRAM for applications
- Supports external serial flash with Quad Peripheral Interface (QPI) mode
- Supports eXecute In Place (XIP) on flash
- Supports interfaces: USB2.0, SDIO, SPI master, SPI slave, I2C, I2S, IR input, UART, AUXADC, PWM, and GPIOs

Audio Subsystem

- Cadence ® Tensilica® HiFi4 processor with 600-MHz clock rate
- Audio Codec with 3 ADC and 2 DAC channels

Secure Boot and Crypto Engine

- Secure boot from serial flash
- Hardware crypto engines including AES, DES/3DES, and SHA

Clock Source

- 26-MHz crystal oscillator
- 32-kHz external crystal oscillator for RTC or internal 32-kHz crystal oscillator

Miscellaneous

- Advanced TDD Wi-Fi/Bluetooth coexistence scheme

1 System Overview

1.1 General Description

The MT7933CT is a highly integrated single chip that features an ARM® Cortex-M33 application processor, a low power 1x1 802.11a/b/g/n/ac/ax dual-band Wi-Fi subsystem, a Bluetooth v5.0 subsystem, an Audio subsystem with Cadence® Tensilica® HiFi4 processor and a Power Management Unit (PMU). The Wi-Fi subsystem and a Bluetooth v5.0 subsystem offer feature-rich wireless connectivity at high standards, and deliver reliable, cost-effective throughput from an extended distance. Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. The MT7933CT is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.
The MT7933CT is based on ARM® Cortex-M33 with floating point microcontroller (MCU) including SRAM/ROM memory. The chip also supports rich peripheral interfaces, including USB2.0, SDIO, SPI master, SPI slave, I2C, I2S, IR input, UART, AUXADC, PWM, and GPIOs.

1.2 Features

1.2.1 Technology and Package

10.6mmx10.6mm BGA package

1.2.2 Power Management and Clock Source

- Integrates high efficiency power management unit with single 3.3V power supply input
- Supports a 26-MHz crystal clock with low power operation in idle mode
- Supports an external 32-kHz crystal oscillator for RTC or internal 32-kHz crystal oscillator for low power sleep mode

1.2.3 Platform

- ARM® Cortex-M33 MCU with FPU with up to 300-MHz clock speed
- Supports up to 96KB for TCM and Cache memory
- Embedded 1MB SRAM
- Embedded 8MB UHS PSRAM for applications
- Supports external serial flash with eXecute In Place (XIP) and on-the-fly AES
- Supports hardware crypto engines including AES, DES/3DES, SHA, ECC, TRNG for network security

- Supports up to 47 general purpose IOs, which are multiplexed with SPI, UART, I2C, I2S, AUXADC, PWM and GPIO interfaces
- Supports 12 DMA channels
- Support USB 2.0 OTG
-

1.2.4 Wi-Fi

- IEEE 802.11 1T1R a/b/g/n/ac/ax 5 GHz and 2.4 GHz bands
- Supports 1x1 20 MHz bandwidth, MCS0~8(256-QAM) in 2.4/5 GHz band
- Support MU-MIMO RX
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- Support Tx LDPC(Low-density parity check)
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- Supports antenna diversity
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1.2.5 Bluetooth

- BT5.2 LE Isochronous Channel
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- Support SCO and eSCO link with re-transmission
- Packet loss concealment
- Channel quality driven data rate adaptation
- Channel assessment and WB RSSI for AFH
- Supports Bluetooth/Wi-Fi coexistence

1.2.6 Audio

- Cadence ® Tensilica® HiFi4 processor with 600 MHz clock speed
- Audio Codec with 3 ADC and 2 DAC channels
- Embedded 256KB SRAM memory for HiFi DSP.
- Support 32KB Instruction and 64KB data cache for HiFi DSP
- Supports Voice Activity Detection (VAD), noise/ echo cancellation and Keyword detection
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1.2.7 Miscellaneous

- Embedded eFuse to store specific device information and RF calibration data
- Advanced TDD mode Wi-Fi/Bluetooth coexistence scheme
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1.3 Block Diagram

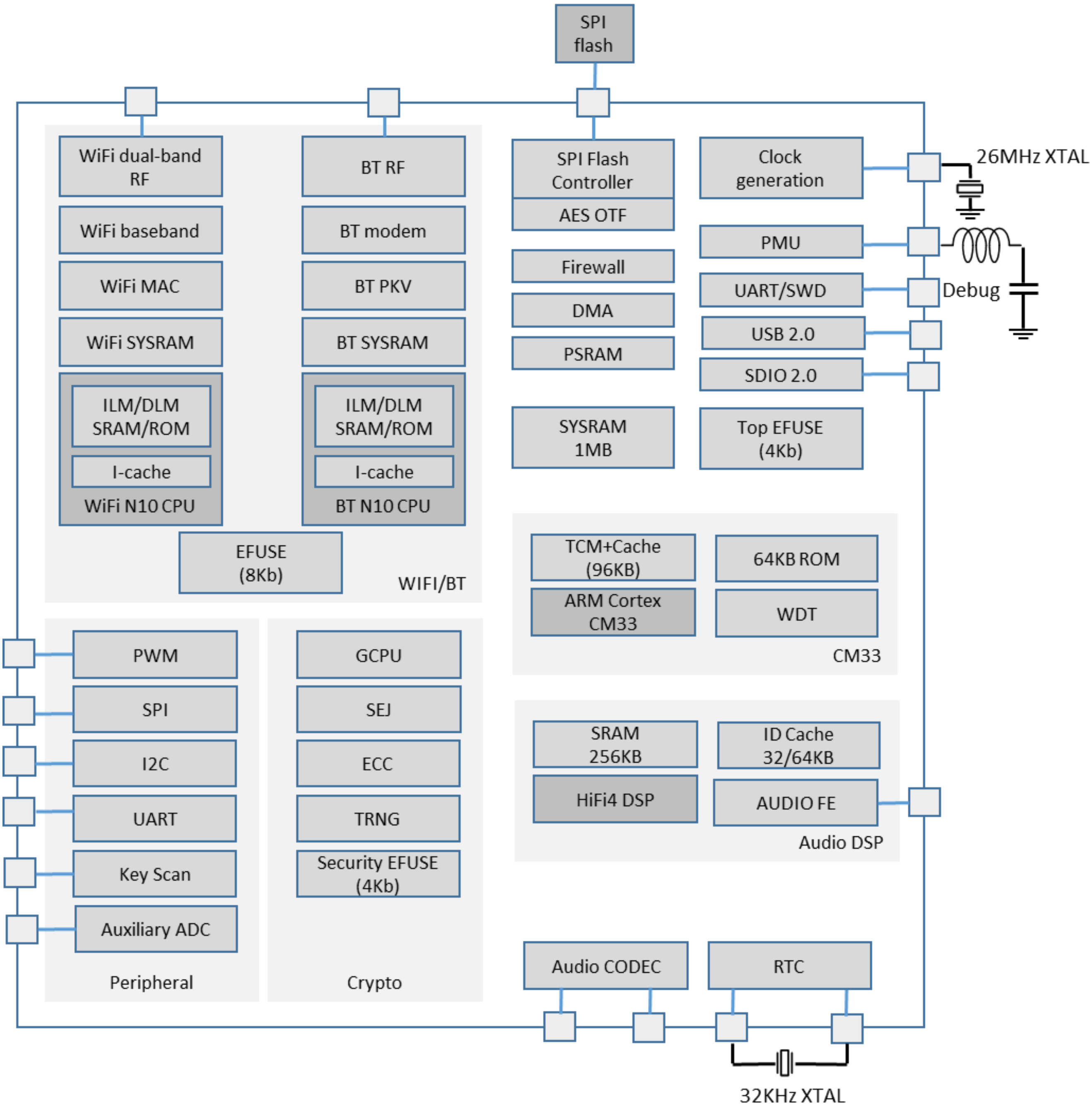


Figure 1-1 MT7933CT System-On-Chip block diagram

2 Functional Description

2.1 Power Management Unit

2.1.1 Introduction

PMU contains two buck converters: BUCK-D(for digital circuit), and BUCK-R (for RF circuit) and four LDOs: PHYLDO (for PLL and USB), AUXLDO (for AUXADC), ALDO (for XTAL) and MLDO (for on-chip memory). Please refer to Figure 2-1. Power grid for more information.

2.1.2 Chip Power Plan

The 3.3V power source directly supplies the PMU, digital IOs (3.3V operation case), and the RF/AIP related circuitry. Please refer to Figure 2-2 for PMU power on sequence with external 32-khz XTAL, and Figure 2-3 for PMU power on sequence without external 32-khz XTAL.

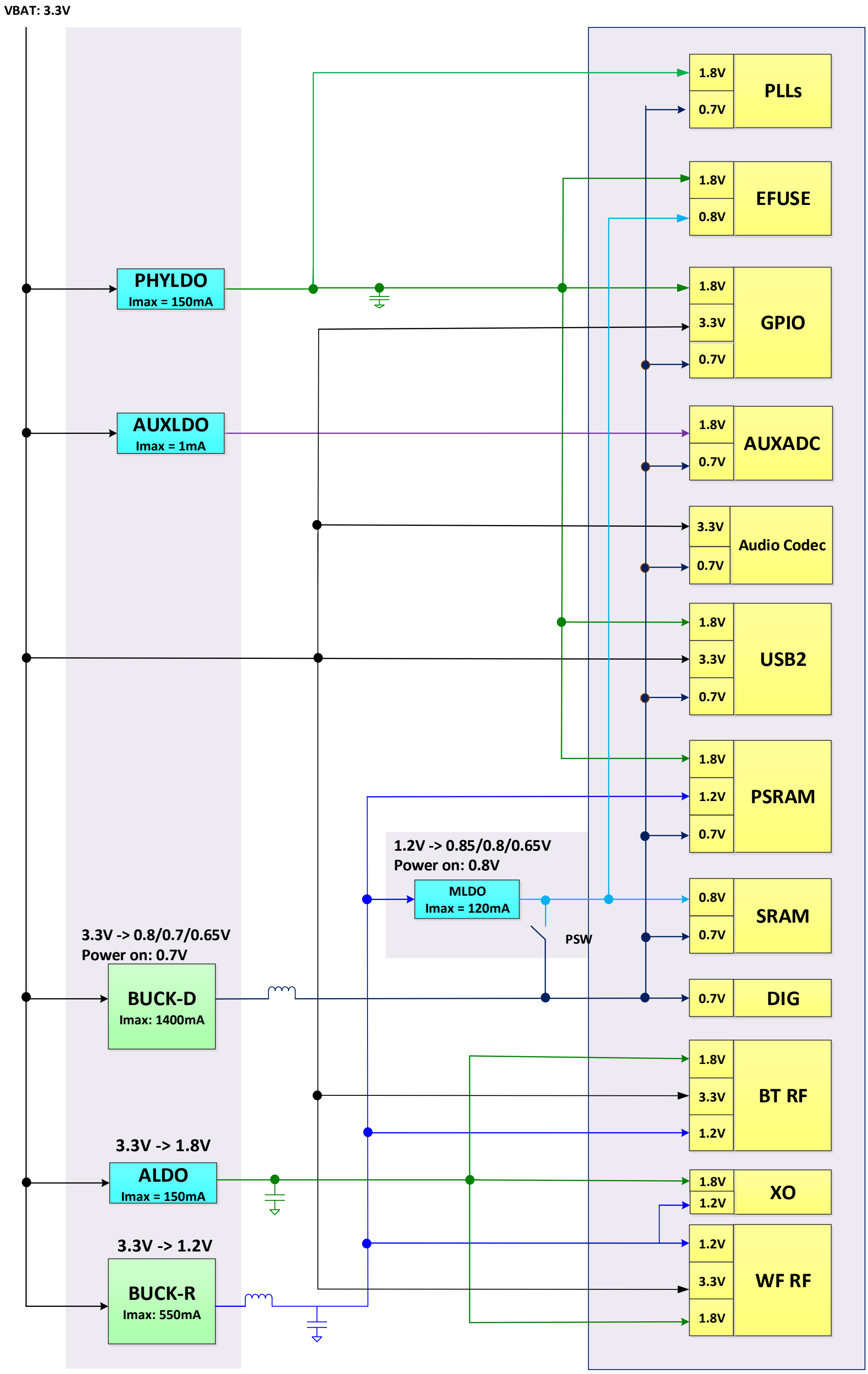
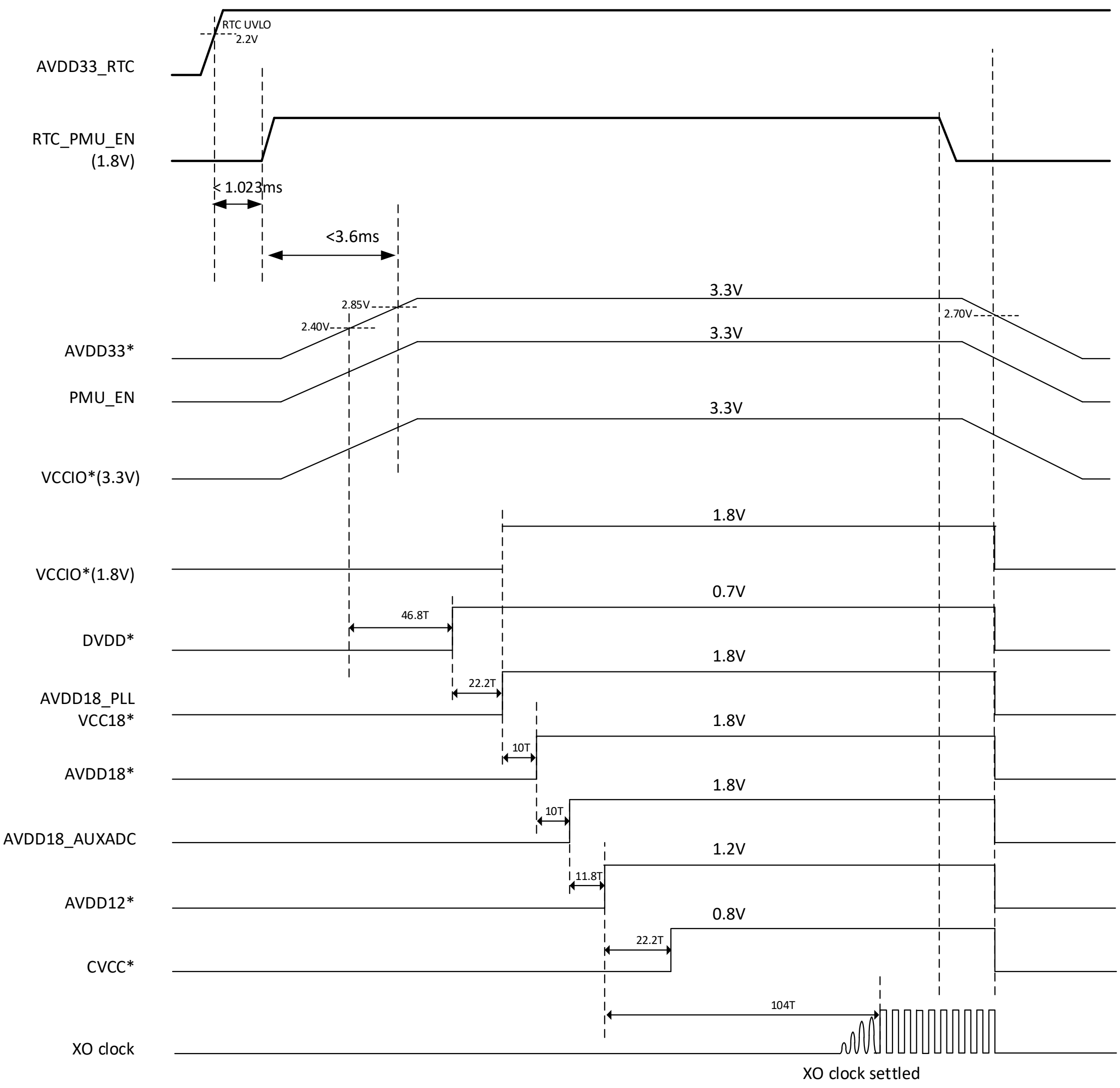
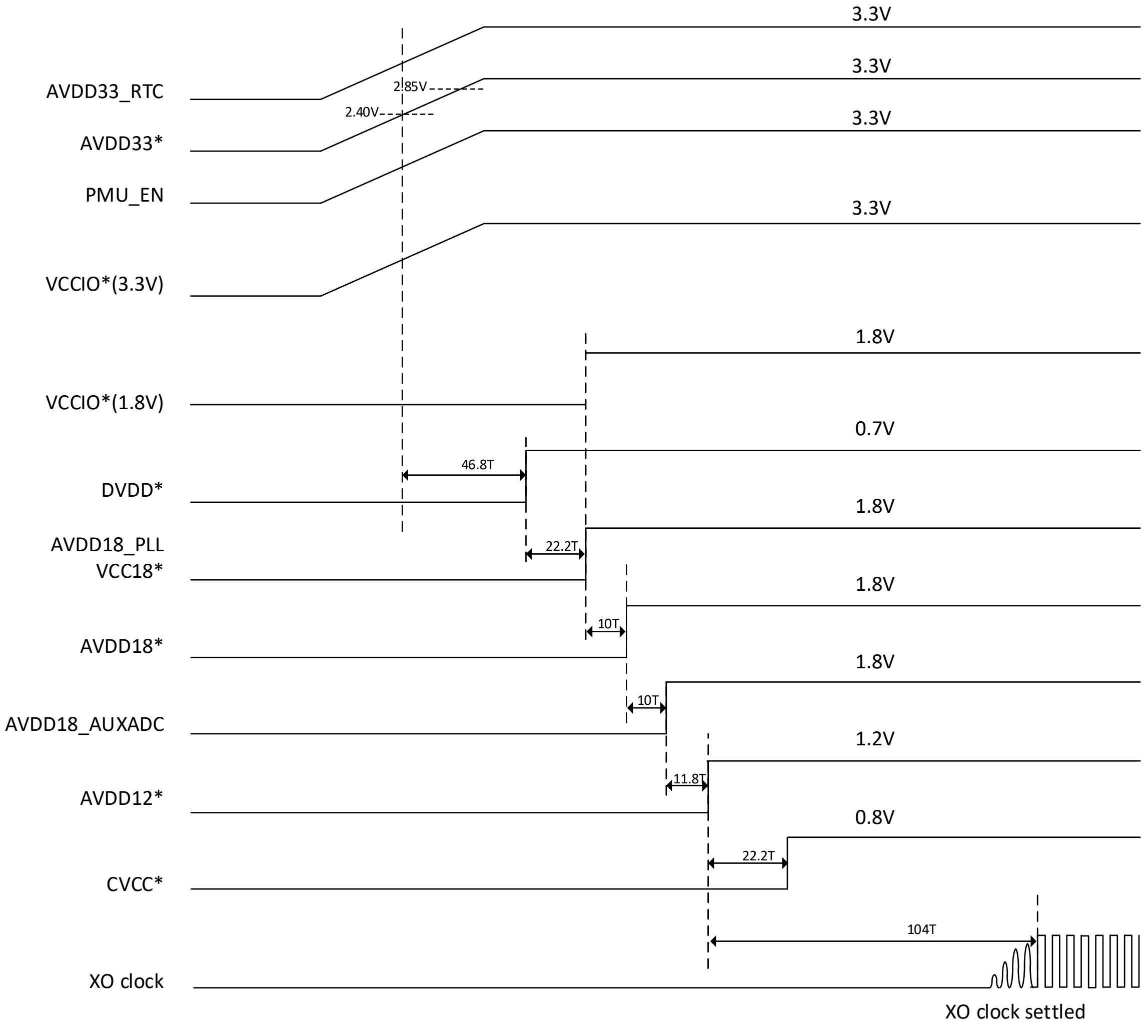


Figure 2-1 Power grid



*BGCLK 12.5kHz ±50% , 1T = max160us, min 53us

Figure 2-2 PMU power on sequence with external 32-khz XTAL



*BGCLK 12.5kHz ±50% , 1T = max160us, min 53us

Figure 2-3 PMU power on sequence without external 32-khz XTAL

2.1.3 Power Performance

Operation Mode		Test Conditions	Current Consumptions (1)	Unit
Power Mode	Scenario			
RETENTION	RETENTION	• RTC Timer • RTC Control Register retention	10	µA
SLEEP	SLEEP_ext_32Khz	• Cortex-M33 in sleep state • 96KB TCM is retained • 1MB SYSRAM is retained • 32-kHz XTAL	800	µA

(1) Conditions: VBAT and VDDIO at 3.3V, temperature at 25°C, typical corner IC, XTAL at 26 MHz

Operation Mode		Test Conditions	Current Consumptions (1)	Unit
Power Mode	Scenario			
ACTIVE	Wi-Fi 2.4G TX	• N10 in active state • Cortex-M33 in active state • 96KB TCM is active • 1MB SYSRAM is active • 8MB PSRAM is active • 26-MHz XTAL	336@CCK 21.5 dBm 308@OFDM 20.5 dBm 222@HT20 17.5 dBm 202@HESU 16.5 dBm	mA
	Wi-Fi 5G TX		510@OFDM 21 dBm 372@HT20 17.5 dBm 354@HESU 16.5 dBm	mA
	Wi-Fi 2.4G RX		38@HT20 MCS0 39@HESU20 MCS8	mA
	Wi-Fi 5G RX		44@HT20 MCS0 47@HESU20 MCS8	mA
ACTIVE & SLEEP	DTIM = 1	• N10 in sleep state • Cortex-M33 in sleep state • 96KB TCM is retained • 1MB SYSRAM is retained • 8MB PSRAM is retained • 32-kHz XTAL	4 (Beacon is 1.6ms)	mW

Note: The chip variation is +/- 25%.

2.1.4 Power State

The MT7933CT platform has several power modes. You could switch the power mode depending on system use case. Please refer to Table 2-1.

Table 2-1 MT7933CT platform power modes

Power Modes	MCU clock	MCU bus	Wi-Fi/BT	Clock	SRAM / PSRAM	Peripheral	Wake Up Source	Wake Up Latency	Power Consumption
Active	300 MHz	Active	Off	PLL / XTAL	Active	On	---		27 mA[1]
Idle	Gated	Active	Off	PLL / XTAL	Active	On	All IRQ	< 1ms	22 mA[1]
Legacy Sleep (PSRAM On)	Gated	Gated	Off	XTAL	Sleep / On	On	All IRQ	< 1ms	16 mA
Deep Sleep	Power off	Power off	Off	RTC	Sleep	Power Off	Restricted IRQ[2]	< 10ms	0.8 mA
RTC Mode	Power off	Power off	Off	RTC	Power off	Power off	RTC_EINT, RTC_TIMER	< 5s	10 uA

[1] The test condition is at 25°C and 3.3V. Power consumed by connectivity is not considered.

[2] List of modules available to signal IRQ as wake up source in deep sleep:

GPT(32K), SDIO slave, EINT, WIFI, BT, UART(CM33), RTC timer, AUDIO, DSP

2.2 System Initialization

MT7933CT system initialization is explained here in two subsections. The chip hardware power-on sequence is described in Section 2.2.1. The system boot up sequence after the secure boot master CM33 takes over the control is described in Section 2.2.3

2.2.1 Chip Power-On

This section explains the chip power-on sequence from 3.3V power supply getting stable to the fundamental chip hardware reset de-assertion (HW_CHIP_RST_B). After this fundamental chip hardware reset de-assertion, secure boot master CM33 takes over the system and boots from its ROM code.
After 3.3V power is stable, the BGCLK (band gap clock) in PMU starts to generate the 25-kHz fundamental clock, the first MT7933CT clock after power on. However, there is +/- 50% uncertainty out of this BGCLK such that this clock is only used for crystal clock control circuit. The power-on sequence is shown in the diagram below and is described in the following steps.

Step 1: 3.3V becomes stable and PMU BGCLK starts to work for PMU initialization
Step 2: After T-pmu (7.7 to 18ms), PMU will be valid and de-assert PMU_RST_N
Step 3: After PMU_RST_N de-assertion, XTAL control circuit will start to work
Step 4: After T-xtal (4.7 to 10.9ms), the crystal clock (XTAL_CLOCK) will be valid
Step 5: T-hwrst (4.7 to 14ms) guarantees that the XTAL_CLOCK is valid before HW_CHIP_RST_B
Step 6: After HW_CHIP_RST_B, IO setting CR will be auto-loaded from eFuse (8ms in 26 MHz)
Step 7: Secure boot master CM33 starts to boot from its ROM

Note that there is a dedicated hardware input pin SYS_RST_N, which is also able to hold the chip reset state. However, this reset will always be de-asserted before PMU_RST_N if the application circuit on the PCB connects this pin to some RC circuit from 3.3V power supply.

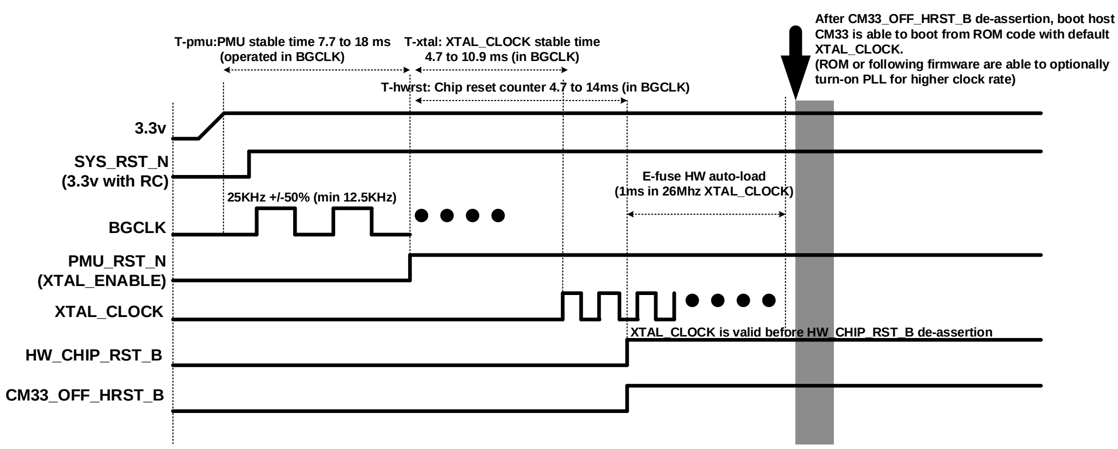


Figure 2-4 Power-On sequence

2.2.2 Bootstrap Function

The section describes the bootstrap function.
The chip modes are sensed from the device pin during power up. After chip reset, the pull configurations are stored in a register and the settings determine the device operation mode.

Table 2-2 MT7933CT strapping pins and modes

Pin name	Pin description	Pin description	Description
GPIO_B_0	GPIO12	Chip Mode Sel	1: Normal mode: Connect 10kΩ to VCCIO_B 0: RSVD
GPIO_B_2	GPIO14	Download and Normal boot Sel	00: CM33 UART download mode 01: CM33 Flash normal boot mode 10: CM33 SDIO download mode 11: CM33 USB download mode e.g.01=GPIO_B_2 connects 10kΩ to GND, GPIO_B_12 connects 10kΩ to VCCIO_B
GPIO_B_12	GPIO24		
SF_QPI_CS	GPIO1	XTAL mode Sel	0: XTAL buffer mode 1: XTAL normal mode

Pins GPIO1, GPIO12, GPIO14, and GPIO24 are used for bootstrap. The system design should follow the following guidelines:

- Those pins shall not be used as input functions because the signals from other devices might affect the values sensed.
- Those pins shall not be used as an open-drain function because the pull-up resistor would affect the values sensed.
- GPIO1 operating voltage is the same as the MT7933CT NOR flash operating voltage.
- GPIO12, GPIO14, and GPIO24 pins also act as GPIO pins; their operating voltages follow VCCIO_B .

2.2.3 System Boot Sequence

The system boot sequence after secure boot master CM33 reset de-assertion is described as below. CM33 will boot up first from BROM, and BROM code will verify security of bootloader and execute code directly on flash by XiP. Besides the boot loader, the flash code also contains the RTOS image for CM33, and the driver and firmware necessary for Wi-Fi, Bluetooth and Audio subsystems. By executing the boot loader, CM33 will verify the security of other flash codes, then jump to RTOS entry point on flash, and fetch the corresponding driver and firmware to enable Wi-Fi, Bluetooth, and Audio subsystems.

The chip initial power state is by default set to ON for Cortex-M33 platform, crypto engine, infra bus and peripherals. But the chip initial state is by default set to OFF for Wi-Fi, Bluetooth and Audio subsystems. Thus, the boot sequence will take care of the power on procedure for those subsystems before enabling them.

2.3 Application Processor Subsystem Cortex-M33

The MCU subsystem consists of a 32-bit MCU, the AHB/APB bus matrix, internal RAM/ROM with ROM patch function, the flash controller and the system peripherals including Direct Memory Access (DMA) engine and the General Purpose Timer (GPT).

2.3.1 CPU

The MT7933CT features an ARM® Cortex-M33 processor, which is the most energy efficient ARM® processor currently available. It supports the clock rates up to 200 MHz when core power is 0.7V and 300 MHz when core power is 0.8V. The MCU executes the Thumb-2 instruction set for optimal performance and code size, including hardware division, single cycle multiplication and bit-field manipulation. The MT7933CT includes a Memory Protection Unit (MPU) in Cortex-M33 MCU to detect unexpected memory access and provide other memory protection features. The MT7933CT also includes FPU in Cortex-M33 MCU.

2.3.2 Cache and Tightly Coupled Memory

The MT7933CT has a cache for Cortex-M33 to improve the efficiency of the code and data fetched from the external flash. The only cacheable memory region is the external flash. The MT7933CT also has a Tightly-Coupled-Memory (TCM), a zero-wait-state memory dedicated to Cortex-M33 and can be accessed by Cortex-M33 exclusively. It is a memory space for the critical code, including interrupt service routines that need to be executed with minimum latency. The total size of cache memory and the TCM is 96KB. We offer four software-configurable options with different cache size, TCM size and cache associativity. You can choose the best option to maximize your application's performance.

The cache system has the following features:

- Write-back (Unit: 4 words)
- Configurable 64/128/256-set, 4-way set associative (8KB/16KB/32KB)
- Each way has 64/128/256 cache lines with 8-word line size (2/4/8KB)
- 20-bit tag memory, including 19-bit high address and 1-bit valid bit
- 2-bit dirty memory. Each dirty bit records the dirtiness of half of the cache line, which is 4 words in this case.

The sizes of TCM and cache can be set to one of the following four configurations:

- 64KB TCM, 32KB cache (4-way, 256-set)
- 80KB TCM, 16KB cache (4-way, 128-set)
- 88KB TCM, 8KB cache (4-way, 64-set)
- 96KB TCM, 0KB cache (no cache)

2.4 Peripherals

2.4.1 Serial NOR Flash Controller

2.4.1.1 Introduction

The MT7933CT provides one serial NOR flash controller for the convenient access to the high-speed serial NOR flash device. The controller supports single-bit SPI serial NOR flash as well as high-performance dual-bit and quad-bit SPI serial NOR flash. The speed of SPI clock could be up to 60 MHz for quad-bit SPI.

2.4.1.2 Features

The serial NOR flash controller supports the following features:

- SPI bus compatible serial interface for common serial NOR flash device
- Map out 512-byte page program buffer, and support multi-page program
- Support SPI mode(single-bit) to transfer page program and 1-byte program
- Support 4-byte address mode, compatible 3-byte address mode
- Support single-bit read, dual output & dual I/O read and quad output & quad I/O read mode
- Read serial NOR flash data through direct read or PIO read mode
- Support serial NOR flash device frequency up to 60 MHz
- For direct read mode, the maximum supported capacity of serial NOR flash device is 2 Gbits. For PIO read modes, the maximum capacity is 4 Gbytes
- Support NOR flash device as follows: MX25U25635FMI, MX25U12835FMI, MX25U6432FM2I, W25Q64JW, W25Q128JW, W25Q256JW, MT25QU128
-

2.4.1.3 Functional Description

The serial NOR flash controller handles all commands, address, data sequence and serial interface protocols. It allows users to read serial NOR flash in two ways: PIO read mode and direct read mode.

1. In PIO read mode, the CPU could program control registers (SNFC_Regs) in a specific sequence and get the serial NOR-flash data through APB. This PIO read mode is usually used for reading data of few bytes.
2. In direct read mode, the CPU could directly read serial NOR flash data through AXI bus by address offset.

2.4.2 Auxiliary ADC Function

2.4.2.1 Functional Description

The MT7933CT features one auxiliary ADC function. The ADC function contains an 12-channel analog switch, a single-end input asynchronous 12-bit SAR (Successive Approximation Register) ADC, dithering function and a digital averaging function.

The digital averaging function can perform on-the-fly averaging function of 1/2/4/8/16/32/64 points.

The ADC features the dithering function to enhance the DNL performance.

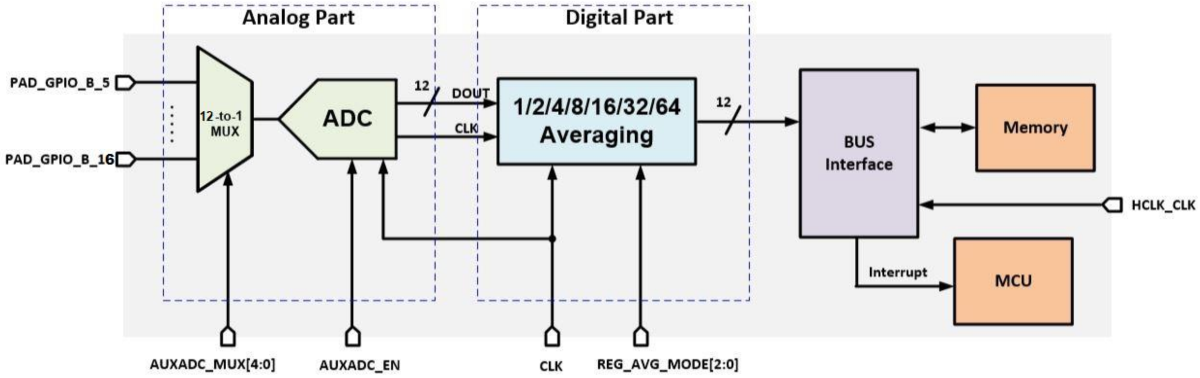


Figure 2-5 Auxiliary ADC block diagram

2.4.2.2 Features and IO

The features of auxiliary ADC are listed below:

- Input channel number: 12 channels
- Sampling and output data rate: 2MS/s (default)
- DNL without dithering and averaging: <±2LSB
- DNL with dithering and averaging: <±1LSB
- Dithering function: 16 levels with step size of 4LSB

The IOs of auxiliary ADC can be set as either analog IO for ADC function or digital IO for GPIO function:

- Analog Mode: Used for ADC application. Input voltage is 1V.

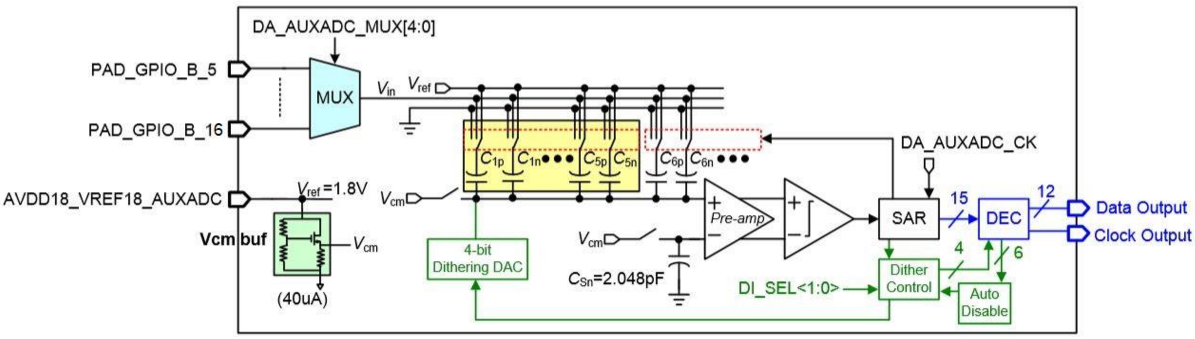


Figure 2-6 Auxiliary ADC analog IP block diagram

2.4.3 SPI Master Controller

2.4.3.1 Functional Description

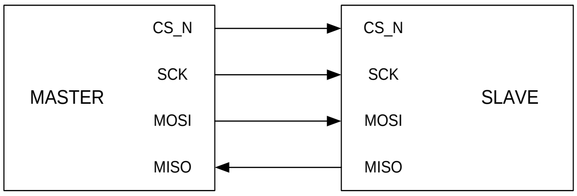


Figure 2-7 Pin connection between SPI master and SPI slave

The SPI interface is a bit-serial, four-pin transmission protocol. The above figure is an example of the connection between the SPI master and SPI slave. The SPI interface controller is a master responsible for the data transmission with the slave.

2.4.3.2 Pin Description

Table 2-3 SPI controller interface

Signal name	Type	Description
CS_N	O	Low active chip selection signal
SCK	O	The (bit) serial clock
MOSI	O	Data signal from master output to slave input
MISO	I	Data signal from slave output to master input

2.4.3.3 Transmission Formats

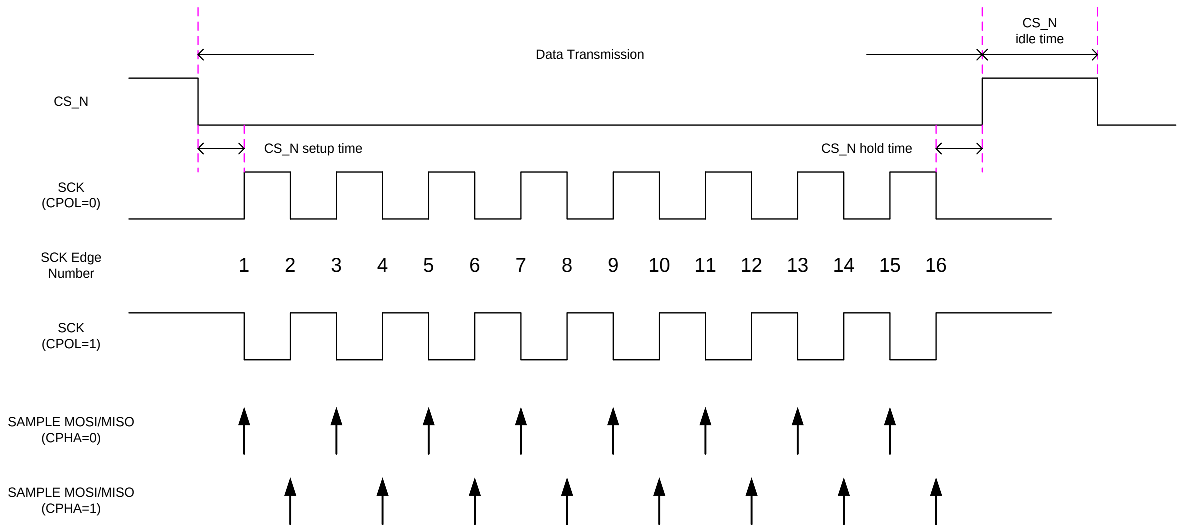


Figure 2-8 SPI transmission formats

The above figure shows the waveform during the SPI transmission. The low active CS_N determines the start point and end point of one transaction. The CS_N setup time, hold time and idle time are also depicted.

CPOL defines the clock polarity in the transmission. Two types of polarity can be adopted, i.e. polarity 0 and polarity 1. The above figure is an example of both clock polarities (CPOL).

CPHA defines the legal timing to sample MOSI and MISO. Two different methods can be adopted.

2.4.3.4 Features

The features of the SPI controller (master) are:

- Configurable CS_N setup time, hold time and idle time
- Programmable SCK high time and low time
- Configurable transmitting and receiving bit order
- Two configurable modes for the source of the data to be transmitted. 1) In Tx DMA mode, the SPI controller automatically fetches the transmitted data (to be put on the MOSI line) from memory. 2) In Tx FIFO mode, the data to be transmitted on the MOSI line are written to FIFO before the start of the transaction.
- Two configurable modes for destination of the data to be received. 1) In Rx DMA mode, the SPI controller automatically stores the received data (from MISO line) to memory. 2) In Rx FIFO mode, the received data keep being in Rx FIFO of the SPI controller. The processor must read back the data by itself.
- Adjustable endian order from/to memory system
- Programmable byte length for transmission
- Unlimited length for transmission. This is achieved by the operation of PAUSE mode. In PAUSE mode, the CS_N signal will keep being active (low) after the transmission. At this time, the SPI controller is in PAUSE_IDLE state, ready to receive the resume command. The state transition is shown in Figure 2-9
- Configurable option to control CS_N deassert between byte transfers. The controller supports a special transmission format called CS_N deassert mode. Figure 2-10 illustrates the waveform in this transmission format.

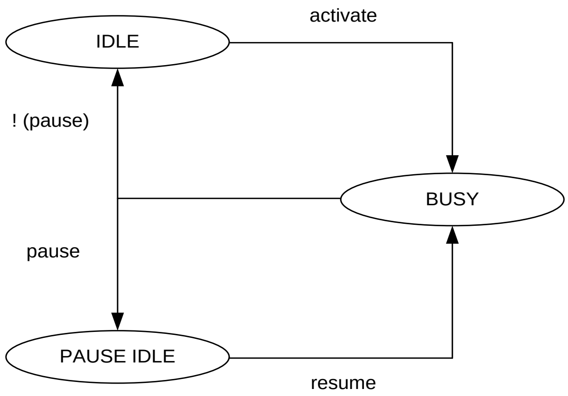


Figure 2-9 Operation flow with or without PAUSE mode

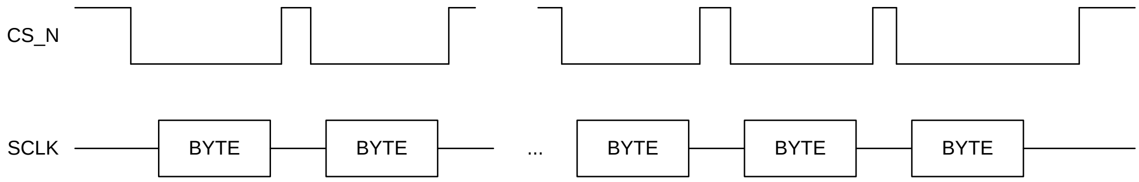


Figure 2-10 CS_N deassert mode

2.4.4 SPI Slave Controller

2.4.4.1 Features

The features of the SPI controller (slave) are listed below:

- The supported SPI_CLK is up to 25 MHz.
- Configurable bit transmitting and receiving order: Two options of bit order – MSB or LSB first
- Four communication modes are available (MODE 0, 1, 2, 3) – that basically define the SCLK edge on which the MISO line toggles and the slave samples the MOSI line. They also define the SCLK signal steady level (namely the clock level, high or low, when the clock is not active). Each mode is formally defined with a pair of parameters called “clock polarity” (CPOL) and “clock phase” (CPHA).

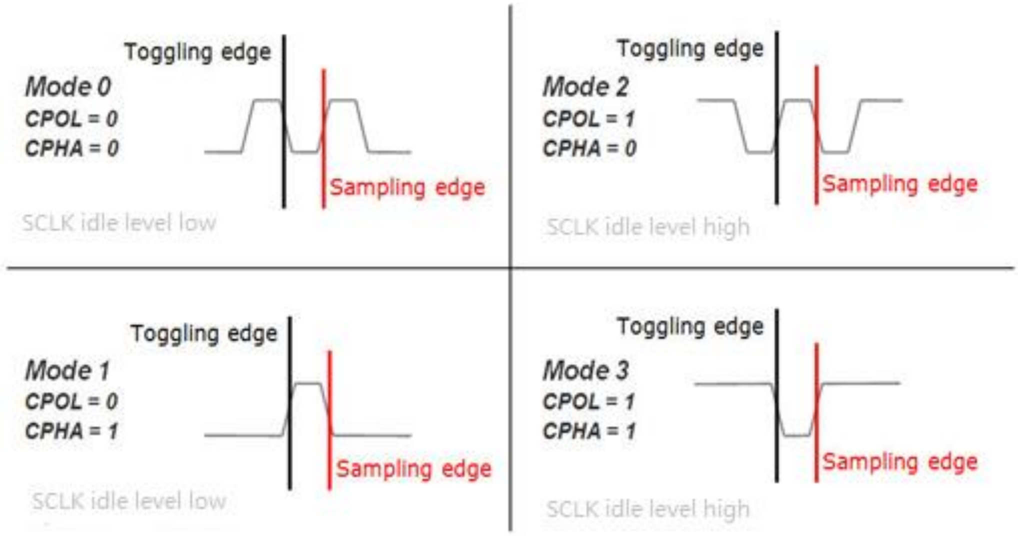


Figure 2-11 Four communication modes waveform

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    - Enable/Disable Transmit and Receive mode
    - Default Tx FIFO data (default is 0x00): If Tx FIFO is empty and the SPI Master wants to get the data from the SPI slave, then the SPI Slave will output configurable constant byte value on MISO, and the default value is 0x00.
    - Rx/Tx FIFO data status: There will be Rx/Tx FIFO pointer and the number of bytes transmitted/received in status register. These can be read for status checking.
    - Interrupt support: There will be Rx full interrupt and transfer done interrupt for indication.
    - Support PIO mode and DMA mode transfer: Both DMA and PIO mode are supported on SPI slave Tx/Rx channel. (Note: Under DMA mode, the value of SPIS_TX_SRC (SPISn Base address+0x0020)[31:0] and SPIS_RX_DST(SPISn Base address+0x001C)[31:0] must be 4-byte aligned)
    - Programmable byte length for transmission: The length of Tx DMA can be programmable from 1 to 1 M bytes.

- Supported Rx DMA byte length is from 1 to (1 M-4) bytes.
- Each FIFO depth of Tx/Rx is 32 x 4 bytes.

2.4.4.2 Pin Description

Description for SPI slave pin is in Table 2-4.

Table 2-4 SPI slave controller interface

Signal Name	Type	Description
CS_N	INPUT	Low active chip selection signal
SCK	INPUT	The (bit) serial clock
MOSI	INPUT	Data signal from master output to slave input
MISO	OUTPUT	Data signal from slave output to master input

2.4.5 SDIO Slave

2.4.5.1 Functional Description

The SD Input/Output (SDIO) card is based on and compatible with the SD memory card. The controller fully supports the SD memory card bus protocol as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0 and SDIO Specification version 2.0.
SDIO provides high-speed data IO with low power consumption. SDIO module provides an SDIO2.0 card interface connected to the host and can support multiple speed modes including default speed mode and high speed mode.

2.4.5.2 Features

- SDIO 2.0 basic features
  - 1-bit and 4-bit SD data transfer modes
  - Default mode: Variable clock rate 0-25 MHz, up to 12.5 MB/sec interface speed (using 4 parallel data lines)
  - High-Speed mode: Variable clock rate 0-50 MHz, up to 25 MB/sec interface speed (using 4 data lines)
- CR and data port access
  - Supports control register (CR) port single read/write access (AHB slave)
  - Supports data port single and burst read/write access (AHB master)
- DMA function
  - One TX channel and two Rx channels
  - Moves TX data from HIF buffer to SYSRAM, TCM
  - Moves RX data or firmware prepared data from SYSRAM, TCM to HIF buffer

2.4.5.3 Block Diagram

The block diagram of the SDIO controller is shown in Figure 2-12

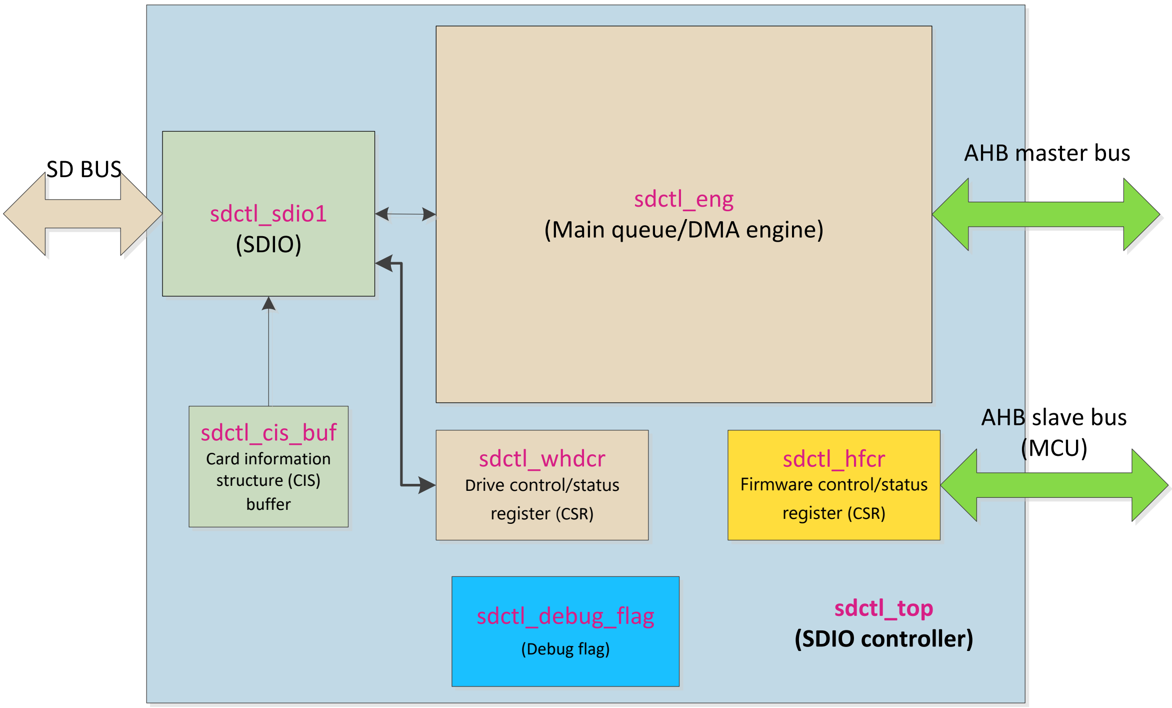


Figure 2-12 SDIO controller block diagram

2.4.5.4 Functions Description

From the external view, the SDIO interface mainly includes the SD bus and AHB master and slave. The AHB master is used for DMA operations and the AHB slave is used for register access from the MCU. The SD bus provides an interface for SD specification.

2.4.5.5 Pin Description

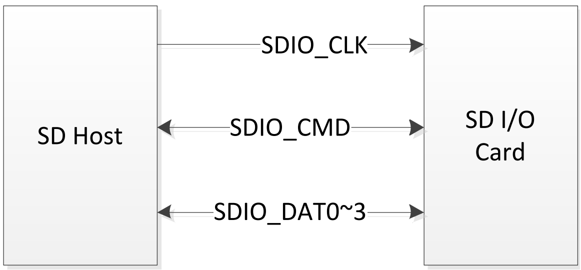


Figure 2-13 Signal connections to 4-bit SDIO cards

Table 2-5 SDIO pin definitions

Pin	Name	SD 4-bit mode		SD 1-bit mode	
1	SDIO_DAT3	DAT[3]	Data line3	N/C	Not used
2	SDIO_CMD	CMD	Command line	CMD	Command line
3	VSS1	VSS1	Ground	VSS1	Ground
4	VDD	VDD	Supply voltage	VDD	Supply voltage
5	SDIO_CLK	CLK	Clock	CLK	Clock
6	VSS2	VSS2	Ground	VSS2	Ground
7	SDIO_DAT0	DAT[0]	Data line0	DATA	Data line
8	SDIO_DAT1	DAT[1]	Data line1 or interrupt	IRQ	Interrupt
9	SDIO_DAT2	DAT[2]	Data line2	RW	Not used

2.4.5.6 SDIO Timing Waveform (3.3V)

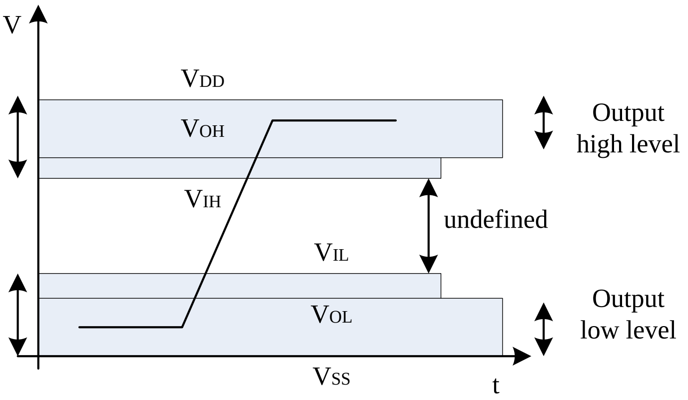


Figure 2-14 Bus signal levels

Table 2-6 Bus signal voltage

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output High Voltage	VOH	0.75*VDD		V	IOH=-2mA VDD min
Output Low Voltage	VOL		0.125*VDD	V	IOL = 2mA VDD min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	Vss-0.3	0.25*VDD	V	

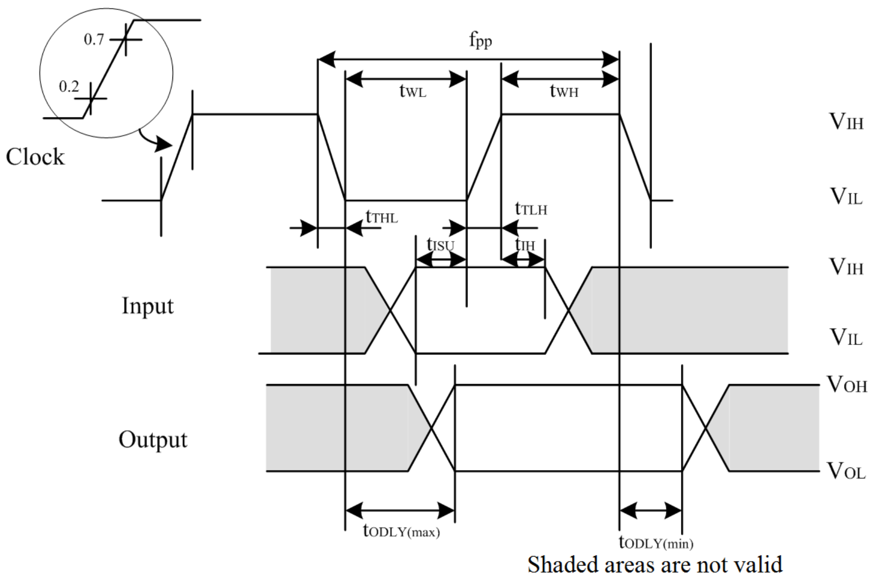


Figure 2-15 Bus timing diagram (default)

Table 2-7 Bus timing parameter values (default)

Parameter	Symbol	Minimum	Maximum	Unit	Remark
Clock CLK (All values are referred to min (VIH) and max (VIL)					
Clock frequency data transfer mode	fPP	0	25	MHz	CCARD ≤ 10 pF (1 card)
Clock frequency identification mode	fOD	0/100	400	kHz	CCARD ≤ 10 pF (1 card)
Clock low time	tWL	10		ns	CCARD ≤ 10 pF (1 card)
Clock high time	tWH	10		ns	CCARD ≤ 10 pF (1 card)
Clock rise time	tTLH		10	ns	CCARD ≤ 10 pF (1 card)
Clock fall time	tTHL		10	ns	CCARD ≤ 10 pF (1 card)
Inputs CMD, DAT (referred to CLK)					
Input set-up time	tISU	5		ns	CCARD ≤ 10 pF (1 card)
Input hold time	tIH	5		ns	CCARD ≤ 10 pF (1 card)
Outputs CMD, DAT (referred to CLK)					
Output delay time during data transfer mode	tOLDY	0	14	ns	CL ≤ 40 pF (1 card)
Output delay time during identification mode	tOLDY	0	50	ns	CL ≤ 40 pF (1 card)

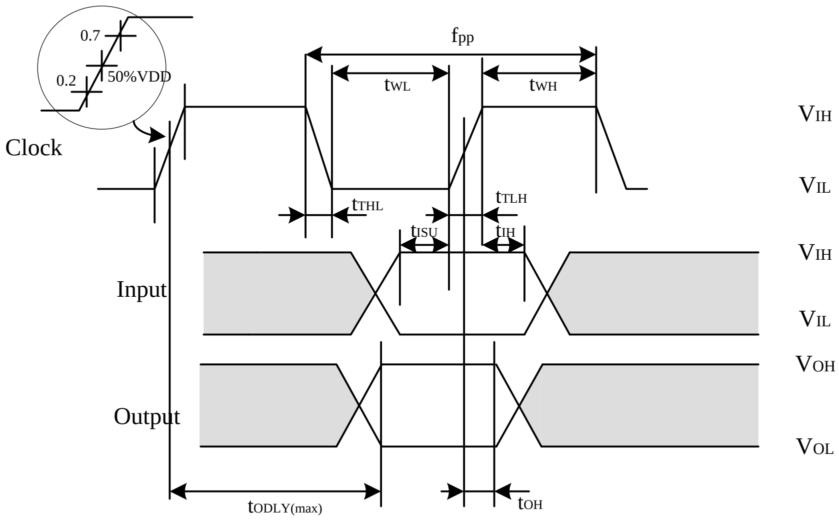


Figure 2-16 High-speed timing diagram

Table 2-8 High-speed timing parameter values

Parameter	Symbol	Minimum	Maximum	Unit	Remark
Clock CLK (All values are referred to min (VIH) and max (VIL)					
Clock frequency data transfer mode	fPP	0	50	MHz	CCARD ≤ 10 pF (1 card)
Clock low time	tWL	7		ns	CCARD ≤ 10 pF (1 card)
Clock high time	tWH	7		ns	CCARD ≤ 10 pF (1 card)
Clock rise time	tTLH		3	ns	CCARD ≤ 10 pF (1 card)
Clock fall time	tTHL		3	ns	CCARD ≤ 10 pF (1 card)
Inputs CMD, DAT (referred to CLK)					
Input set-up time	tISU	6		ns	CCARD ≤ 10 pF (1 card)
Input hold time	tIH	2		ns	CCARD ≤ 10 pF (1 card)
Outputs CMD, DAT (referred to CLK)					
Output delay time during data transfer mode	tOLDY		14	ns	CL ≤ 40 pF (1 card)
Output hold time	tOH	2.5		ns	CL ≥ 40 pF (1 card)
Total system capacitance for each line (1)	CL		40	pF	1 card

(1) In order to satisfy the serving time, the host shall drive only one card.

2.4.6 I2C

2.4.6.1 Introduction

There are two I2C master channels in the MT7933CT with the same HW architecture. I2C is a two-wire serial interface with two signals, SCL and SDA. SCL is a clock signal driven by the master. SDA is a bi-directional data signal that can be driven either by the master or by the slave. This generic controller supports the master role and conforms to the I2C specification.

2.4.6.2 Features

The main supported features of I2C Master are as follows:

- I2C compliant master mode operation
- Adjustable clock speed for Fast-mode Plus
- 7-bit address
- Clock stretching feature
- START/STOP/repeated START conditions
- I2C_FIFO mode
- DMA transfer mode
- Multi-write per transfer

- Multi-read per transfer
- Multi-transfer per transaction
- Combined format transfer with length change capability
- Multi-transfer with repeated START condition

2.4.6.3 Block Diagram

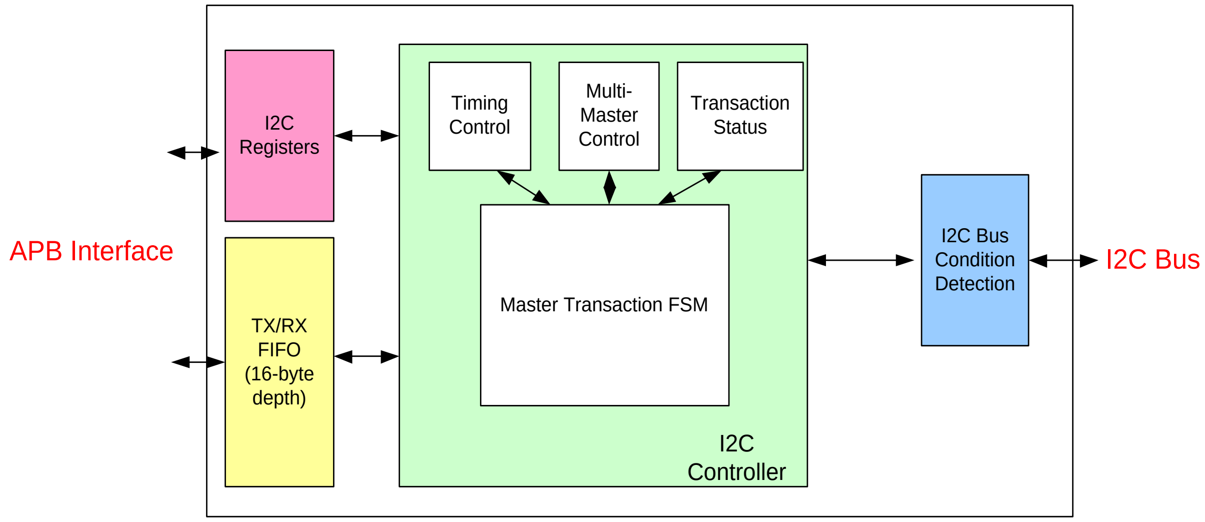


Figure 2-17 Block diagram of I2C

- I2C Registers: I2C configuration and status registers.
- Tx/Rx FIFO: Store the data to be sent to I2C slave or the data received from I2C slave.
- Master Transaction FSM: I2C master finite-state machine used to indicate the current transfer stage.
- Timing Control: Control the frequencies of SCL according to the configuration of CLOCK_DIV , SAMPLE_CNT_DIV and STEP_CNT_DIV.
- Multi-Master Control: Execute arbitration when multiple masters exist on the I2C bus.
- Transaction Status: Record the number of bytes that has been transferred and the number of transfers that has been done. It can be used to judge if all transactions have been completed.
- I2C Bus Condition Detection: Detect START/STOP/repeated START conditions and clock stretching on the I2C bus.

2.4.7 UART

2.4.7.1 Introduction

The UART controller provides full duplex serial communication channels between the MT7933CT chip and external devices. The UART controller has M16C450 and M16550A operation modes, which are compatible with a range of standard software drivers. The extensions are designed to be broadly software compatible with 16550A variants, but certain areas offer no consensus.

In common with the M16550A, the UART controller supports word lengths from 5 to 8 bits, an optional parity bit and one or two stop bits, and this word length is fully programmable by a CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, along with separate transmission and received FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided. The UART_TOP also includes two DMA handshake lines which are used to indicate when the FIFOs are ready to transfer data to the CPU. Interrupts can be generated from any of the several sources.

After hardware reset, the UART controller is in M16C450 mode. Its FIFOs can be enabled and the UART controller can enter M16550A mode. The UART controller adds further functionality beyond M16550A mode. Each of the extended functions can be selected individually under software control.

2.4.7.2 Features

- Provide 4 channels of UART controller
- UART_TOP0, UART_TOP1 and CM33_UART are 4-pin (TX, RX, CTS, RTS) UART_TOP channel
- DSP_UART is a 2-pin (TX, RX) UART_TOP channel
- Support both M16C450 and M16550A operation modes
- Compatible with standard software drivers
- Transfer system: Asynchronous
- Data length: 5 to 8 bits
- Hardware flow control: CTS/RTS-based automatic transmission and reception of control
- Software flow control: Use special character XON/XOFF to do software flow control
- Baud rate is programmable from 300 bps to 3 Mbps
- Baud rate error: Less than 0.25 %
- Interrupt request: Receive interrupts/transmit interrupts
- Data transfer: DMA (Transmit/Receive) transfer is supported

2.4.8 PWM

2.4.8.1 Functions Description

The MT7933CT features 12 generic PWMs to generate pulse sequences with programmable frequency and duration for LCD, vibrators, and other devices.

The PMU features three configurable pattern options.

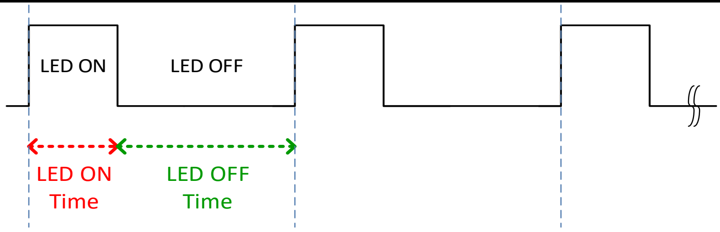
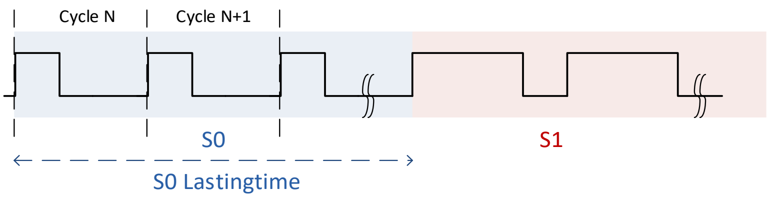
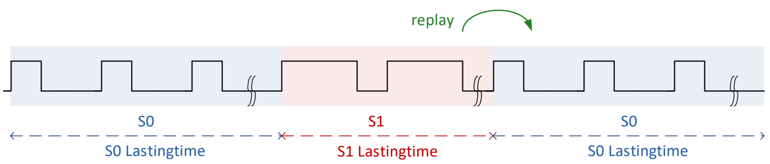
Mode	Description	Waveform
1	Basic PWM: LED ON time (duration) and LED OFF time (duration) are configurable.	
2	Two-State PWM: There are two configurable states (S0 and S1) for PWM LED.	
3	Two-State replay mode: Users can set replay mode with specified S1_Lasting_Time. PWM LED would act as [S0 -> S1 -> S0 -> S1 -> S0 ….] with period time of (S0_Lasting_Time + S1_Lasting_Time)	

Figure 2-18 PWM patterns

2.4.9 USB

2.4.9.1 USB Host Controller

2.4.9.1.1 Introduction

The MT7933CT features a USB host controller which provides one USB 2.0 host port. The operation model of the host functional blocks conforms to eXtensible Host Controller Interface (xHCI) for Universal Serial Bus (USB) specification.

2.4.9.1.2 Features

- The hardware supports USB 2.0 with LS (Low-speed) 1.5 Mbps/FS (Full-speed) 12 Mbps/HS (High-speed) 480 Mbps
- Embedded USB 2.0 PHY with 16-bit/30-MHz UTMI interface
- AHB interface for register access
- AXI interface for DMA access
- xHCI-based host controller
- LPM (Lower Power Management) on the USB 2.0 port
- Dedicated DMA channel for USB 2.0 data transfer
- Supports all USB compliant data transfer types with control/bulk/interrupt/isochronous transfer and split transactions
- Compatible with USB 2.0 hub
- Supports up to 15 devices
- Supports up to 64 endpoints

2.4.9.1.3 Block Diagram

Figure 2-19 illustrates the architecture of the USB host. It has one port configured as USB 2.0 host mode. All the resources of endpoint and device are handled by the xHCI controller. The software could dynamically allocate resources for different ports and turn on or off each port separately. The xHCI controller controls the exchange of data and PHY, and controls DMA to write data to or read data from EMI.

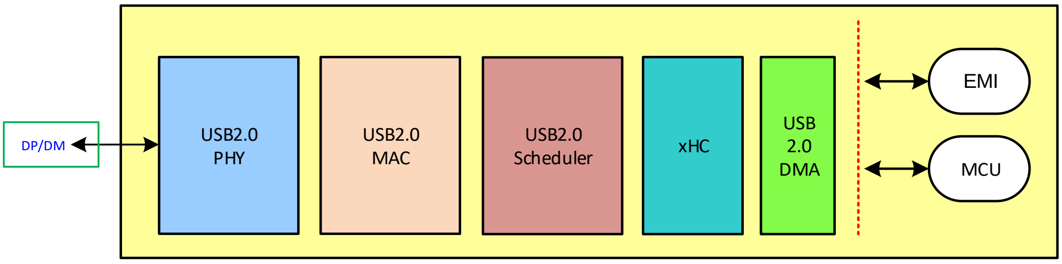


Figure 2-19 USB host architecture

2.4.9.2 USB Device Controller

2.4.9.2.1 Introduction

The MT7933CT provides a high performance USB 2.0 device port that supports USB 2.0 High-/Full-Speed (480 Mbps/12 Mbps). The feature list and functional block diagram are provided in the following sections.

2.4.9.2.2 Features

- The USB 2.0 device controller supports the following features:
  - The hardware supports USB 2.0 High-/Full-Speed
  - Embedded USB 2.0 PHY with 16-bit / 30-MHz UTMI interface
  - AHB interface for register access
  - AXI interface for DMA
  - Embedded queue management function with scatter/gather DMA capability
  - Lower Power Management (LPM) on the USB 2.0 port
  - Hardware-configurable number of OUT Endpoints and IN Endpoints, with each up to 8
  - Software-configurable FIFO size allocated for each endpoint separately
  - Software-configurable transfer type to Bulk/Interrupt/Isochronous for each endpoint

2.4.9.2.3 Block Diagram

Figure 2-20 illustrates the architecture of the USB 2.0 device function.

The device controller includes USB 2.0 PHY, USB 2.0 MAC, BMU (Buffer Management Unit), QMU (Queue Management Unit), and DMA. QMU and BMU, instead of MCU, perform DMA control. The data is received via PHY, USB 2.0 MAC handle, QMU/BMU configuration DMA, and then written to EMI through DMA. For data transmission, QMU/BMU configuration DMA reads data from EMI through DMA, after handling by USB 2.0 MAC, data is sent through the PHY.

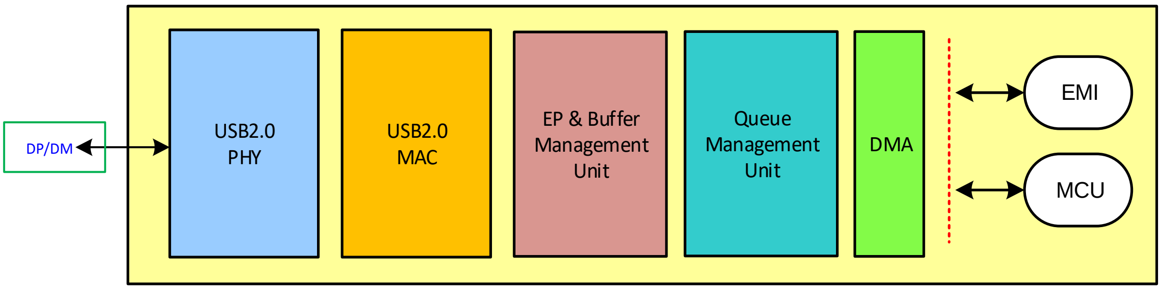


Figure 2-20 USB device architecture

2.4.10 DMA

Direct memory access (DMA) is used to transfer data between memory and memory as well as memory and peripherals without MCU interventions.

2.4.10.1 Command Queue (CQ) DMA

The purpose of CQ_DMA is to perform data transfer between memory and memory without CPU interventions.

The supported features of CQDMA are as below:

- Up to three channels of simultaneous data transfer are supported.
- Comply with the system bus (AXI).
- Two out-standings for three channels
- Source or destination address fix mode
- Source or destination address-wrapping mode
- Source and destination address-increment mode
- Fix-pattern mode
- Bandwidth limiter
- TrustZone
- Round-Robin (RR) for scheduling scheme

2.4.10.2 Application Processor (AP) DMA

The purpose of APDMA is to perform data transfer between memory and peripherals.

The supported features of APDMA are as below:

- Up to 9 channels of simultaneous data transfer are supported.
- Comply with the system Bus (AXI)
- TrustZone
- Interrupt notification
- Round-Robin (RR) for scheduling scheme

There are 2 types of DMA channels supported in MT7933CT.

- Peripheral DMA: The behavior of Peripheral DMA is like that of CQ-DMA. The major difference is that the source or destination is peripherals FIFO, not memory.
- Virtual FIFO DMA (VFF DMA): It's a peripheral DMA with an additional FIFO control engine. It is used to provide the buffering capacity for peripherals.

2.4.10.2.1 Peripheral DMA

The behavior of Peripheral DMA is like that of CQ-DMA. The major difference is that the source or destination is peripheral FIFO, not memory. And there are handshaking signals (REQ / ACK) between DMA and peripheral. Because of handshaking signals, the DMA channels with corresponding peripheral channels are fixed.

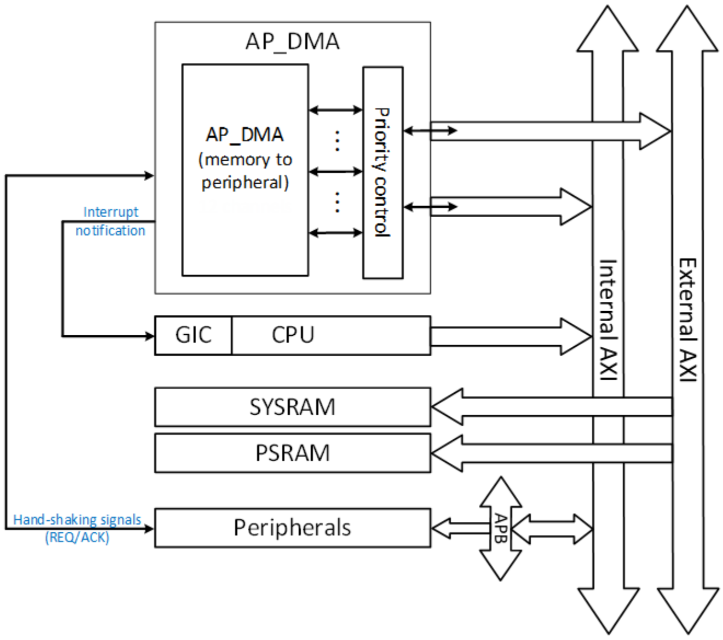


Figure 2-21 APDMA block diagram

2.4.10.2.2 Virtual FIFO

Virtual FIFO DMA is designed to offload the control of the serial interface. The difference between the virtual FIFO DMA and the peripheral DMA is that the virtual FIFO DMA contains an additional FIFO controller.
VFF is like the ring buffer, and uses two address pointers (VFF_WPT/VFF_RPT) to control VFF condition.
According to these two address pointers, two symbols are defined (VFF_VALID_SIZE/VFF_LEFT_SIZE) to represent the valid data and available space in VFF.
The figure below illustrates the operations of virtual FIFO DMA used for UART RX.

(1) READ: DMA controller reads data from UART and increments the WRITE pointer of the FIFO controller.
(2) WRITE; DMA controller writes data that was area from UART to SRAM in the area defined before enabling the virtual FIFO.
(3) READ: MCU reads data when FIFO is not empty and the amount of data is over a pre-defined threshold. The read transaction will be finished only when DMA controller reads back the data from SRAM.
(4) READ: DMA controller reads data from SRAM and increments the READ pointer of the FIFO controller.

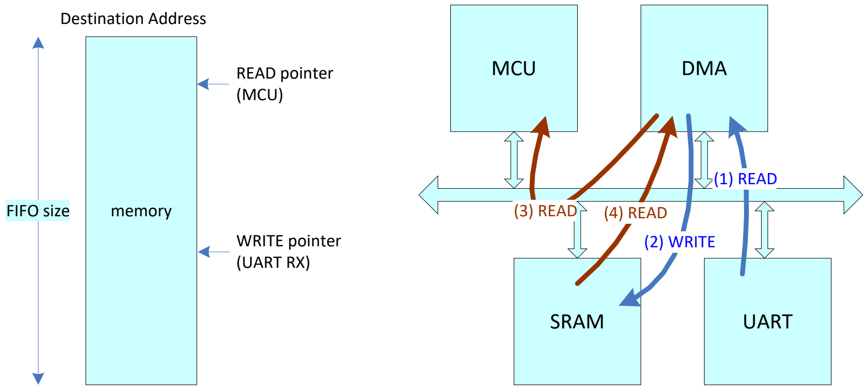


Figure 2-22 Virtual FIFO concept

2.4.10.2.3 APDMA Channels and Priority Control

There are totally 7 virtual FIFO DMA channels and 2 peripherals DMA channels in the MT7933CT.

Table 2-9 DMA type for hardware IP

Hardware IP	DMA Type
Radio (Bluetooth)	Virtual FIFO DMA x 2
UART (x2)	Virtual FIFO DMA x 4
AUXADC	Virtual FIFO DMA x 1
I2C	Peripheral DMA x 2

2.4.11 GPT

2.4.11.1 Introduction

The Application Processor X General Purpose Timer (APXGPT) module includes five 32-bit GPTs and one 64-bit GPT. Each GPT supports four operation modes, which are ONE-SHOT, REPEAT, KEEP-GO and FREERUN. Each GPT can be operated on one of the two clock sources, RTC clock (32.768 kHz) or system clock (13 MHz).

2.4.11.2 Features

Table 2-10 provides the detailed information about the four operation modes for the GPT, ONE-SHOT, REPEAT, KEEP-GO and FREERUN.

Table 2-10 Operation mode of GPT

Mode	Auto Stop	Interrupt Supported	Counting Behavior	When GPTn_COUNT equals GPTn_COMPARE	Example: Compare value is set to 2 (The bold value means interrupt asserted)
ONE-SHOT	Yes	Yes	The GPT stops counting when GPTn_COUNT equals GPTn_COMPARE	EN is reset to 0	0,1,**2**,2,2,2,2,2,2,2,2,2,...
REPEAT	No	Yes	The GPT count is reset to 0 when GPTn_COUNT equals GPTn_COMPARE	Count is reset to 0	0,1,**2**,0,1,**2**,0,1,**2**,0,1,**2**...
KEEP-GO	No	Yes	The GPT count is reset to 0 when overflow occurs		0,1,**2**,3,4,5,6,7,8,9,10,...
FREERUN	No	No	The GPT count is reset to 0 when overflow occurs		0,1,2,3,4,5,6,7,8,9,10,...

Note:

Each timer's operation is independent and can be programmed to select the clock source, RTC clock (32.768 kHz) or system clock (13 MHz). After the clock source is determined, the division ratio of the selected clock can be programmed. The division ratio can be fine-granulated as 1 to 13 and coarse-granulated as 16, 32 and 64.

2.4.11.3 Block Diagram

APXGPT consists of five sets of 32-bit GPTs and one set of 64-bit GPTs.
When the GPT triggers an IRQ, it will also issue a wakeup signal to "Sleep Control", and then “Sleep Control” can wake the MCU if the MCU is in sleep mode.

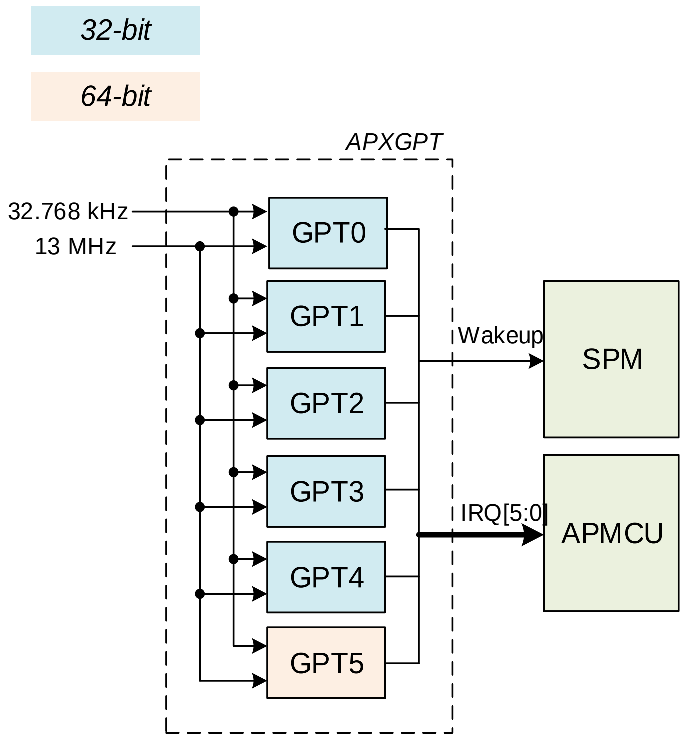


Figure 2-23 Block diagram of APXGPT

2.4.11.4 Theory of Operations

For the GPT5 64-bit timer, the read operation of the 64-bit timer value will be separated into 2 APB reads since an APB read is of 32-bit width. To perform the read operation of 64-bit timer value, the lower word should be read first and then the higher word. The read operation of the lower word will freeze the “read value” of the higher word but will not freeze the timer counting. This ensures that the separated read operation acquires the correct timer value.

To program and use the GPT, please note:
The counter value can be read at any time when the clock source is system clock.
The counter value can be read at any time even when the clock source is RTC clock.
The comparative value can be programmed at any time. When the comparative value is rewritten during count operation, the counter will be reset to 0 and restart counting.

2.4.12 WDT

2.4.12.1 Introduction

The MT7933CT features a watchdog timer (WDT) for the Arm Cortex-M33 processor (referred to as CM33 in this document). CM33_WDT is the watchdog timer for the Cortex-M33 processor. When the Cortex-M33 processor hangs due to some malfunctions, the watchdog timer is used to generate system alarm and trigger whole chip reset.

2.4.12.2 Functional Description

The WDT provides the counter with the clock source of 32 kHz and asserts interrupt when needed. There is an interrupt counter, and it can operate as follows:

- One-shot mode: the timer stops when the timer counts down to zero.
- The timer counts from a programmable initial value and asserts interrupt when counting to zero. The interrupt will be level active low. The unit of the counter can be 1 x 32 kHz cycle.

  The WDT provides two ways to generate the WDT event.
- Triggered by the time-out event to configure WDT HW reset mode.
- The WDT has an 11-bit counter and uses the 32-kHz clock. The software regularly restarts the timer to prevent it from expiring. If the timer fails to restart the WDT, it will expire and generate a WDT event.
- The programmable period length is 32ms*(1~2048) which is ranged from 32ms to 65.5s.
- Triggered by software programming to write SW reset KEY.

2.4.12.3 Event Notification for CM33

The WDT provides the following options when a WDT event is generated.

- Trigger whole chip reset
- Interrupt itself

  Note: The reset whole chip option is included in top chip reset register space.

The WDT module can only be reset by the external reset (SYS_RST_N) and the PMU reset. Some WDT control registers feature a key protection mechanism to prevent unintentional access.

2.4.13 GPIO

2.4.13.1 Overview

The MT7933CT platform offers 47 General-Purpose Input/Output (GPIO) pins. By setting the control registers, the MCU software can control the direction and the output value of the GPIO pins and read the input value of these pins. The GPIO pins and GPO (General-Purpose Output) pins are multiplexed with other functions to reduce the pin count.

The clock to send data outside the chip is software configurable. There are six clock-out ports and each clock-out port can be programmed to output the appropriate clock source. In addition, when two GPIO pins function for the same peripheral IP, the smaller GPIO serial number has higher priority over the bigger one.

Figure 2-24 shows the block diagram of the GPIO controller in the MT7933CT.

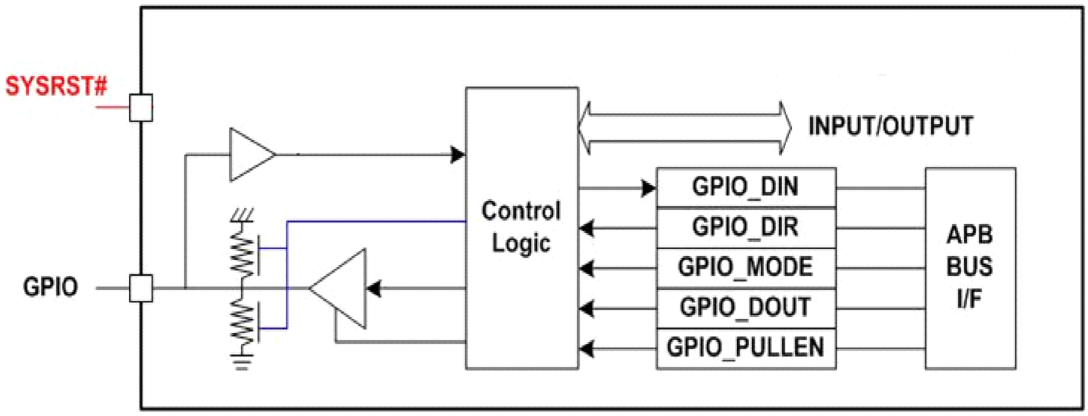


Figure 2-24 MT7933CT GPIO controller

2.4.13.2 I/O Pull up or Down Control Truth Table

All MT7933CT GPIO pins support both 1.8V and 3.3V IO power and different Pull up/Pull down resistors can be selected as Table 2-11.

Table 2-11 PU/PD resistance Spec

E	PUPD	R1	R0	R Value of 1.8V/3.3V IO Power
0	0	0	0	High-Z
0	0	0	1	PU10Kohm
0	0	1	0	PU50Kohm
0	0	1	1	PU10Kohm//50Kohm
0	1	0	0	High-Z
0	1	0	1	PD10Kohm
0	1	1	0	PD50Kohm
0	1	1	1	PD10Kohm//50Kohm
1	X	X	X	High-Z

2.5 Audio System

2.5.1 Audio Digital Signal Processor (DSP)

2.5.1.1 Introduction

DSP is responsible for running operating system and application programs. It comprises:

- One-core Cadence HiFi4 Audio Engine DSP
- AXI3 Bus Interface Unit (in-house MTK Bus)
- SPM control

Cadence's HiFi4 Audio Engine is a highly optimized audio processor geared for efficient execution of audio and voice codecs and pre/post-processing modules.

The processor goes beyond the HiFi3 with support for four 32x32-bit MACs, some support for 72-bit accumulators, limited ability to support eight 32x16-bit MACs, a fourth VLIW slot and the ability to issue two 64-bit loads per cycle. There is an optional floating point unit available, providing up to four single-precision IEEE floating point MACs per cycle. The extra resources provide significant performance improvements as compared to the HiFi3, particularly on pre/post-processing algorithms.

The HiFi4, a Single-Instruction/Multiple-Data (SIMD) processor, has the ability to work in parallel on two 32-bit data items or four 16-bit data items. HiFi4 is a VLIW architecture, supporting the execution of four operations in parallel.

2.5.1.2 Features

One-core Cadence's HiFi4 DSP operates at 300 MHz (0P7V)/600 MHz (0P8V), including:

- 32KB L1 I-cache
- 64KB L1 D-cache
- Pre-fetch buffer, I-cache, D-cache, ITag, and Dtag don't support data retention
- 32x32-bit MACs
- JTAG
- 25 interrupts
- Support SPM to control power sequence
- UART

2.5.2 Audio Channels

2.5.2.1 Functional Description

The audio system provides the ability to exchange audio data. The interfaces are listed as follows:

- Support 1* master 2-ch I2S output sample rates: 8 kHz to 192 kHz; bit resolution up to 32 bits
- Support 1* master/slave 2-ch I2S input sample rates: 8 kHz to 192 kHz; bit resolution up to 32 bits
- Support one built-in master TDM input interface: supported sampling rates include 8, 12, 16, 24, 32, 48, 96, 192 kHz; channel number up to 8
- Support 2-ch DMIC Pulse Density Modulation (PDM) interface x 2: one wire mode; 8, 16, 32, 48 kHz; 24 bits
- 2-ch built-in internal audio DAC: 8 to 48 kHz
- 3-ch built-in internal audio ADC: 8, 16, 32, 48 kHz; support dedicated HW gain: -75 dB to 24 dB
- Support 1-pair stereo general-purpose ASRC for sampling rate converter and salve mode clock tracking
- Support 2-ch HW gain for fade in and fade out
- Support 16-ch channel merge
- APLL x 1, can support two clock rates at the same time.
- Built-in 64KB audio internal SRAM

2.6 Interrupt

2.6.1 Introduction

The MT7933CT embeds an interrupt controller, which is composed of an NVIC (Nested Vectored Interrupt Controller), a WIC (Wakeup Interrupt Controller) and a de-bounce circuit. The WIC and de-bounce circuits are in the Always-On domain. All internal or external interrupts are connected to the WIC as well as to the NVIC; thus, each interrupt signal can serve as a wakeup source for the CM33 processor. And these interrupt sources could be level or edge triggered by configuration.

2.6.2 Block Diagram

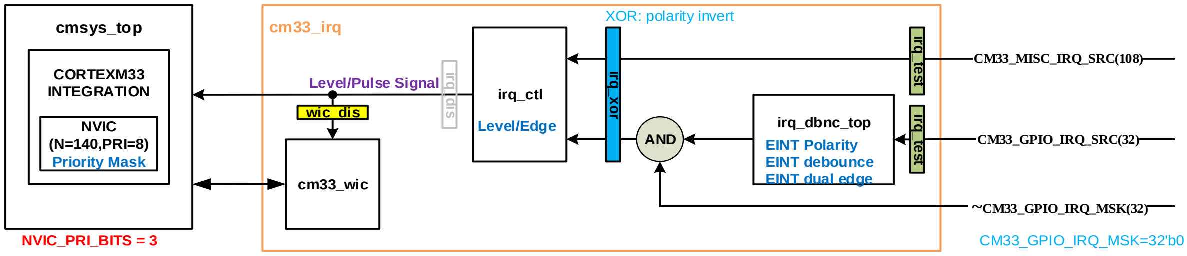


Figure 2-25 CM33_IRQ block diagram

2.6.3 Interrupt Table

Table 2-12 CM33 interrupt

MCU IRQ NUM	Interrupt Name	Interrupt Description	Polarity	Edge / Level	EINT
0	wic_int_wake_up	WIC wakeup interrupt to CM33	H	edge(HW) level(SW)	X
1	Reserved				
2	Reserved				
3	~wdt_irq_b0	CM33 WDT interrupt (wdt_irq_b[0])	H	edge	X
4	~uart_irq_b	CM33 UART interrupt	H	level	X
5	infra_bus_int	Infra bus error interrupt	H	level	X
6	dbgsys_CDBGPWRUPREQ	CoreSight debug power up req	H	level	X
7	dbgsys_CDBGPWRUPACK	CoreSight debug power up ack	H	level	X
8	~wdt_irq_b1	CM33 WDT interrupt (wdt_irq_b[1])	H	level	X
9	dsp_to_cm33_irq	DSP to CM33 IRQ	H	level	X
10	~apxgpt_irq_b0[0]	GPT_32_0	H	level	X
11	~apxgpt_irq_b0[1]	GPT_32_1	H	level	X
12	~apxgpt_irq_b0[2]	GPT_32_2	H	level	X
13	~apxgpt_irq_b0[3]	GPT_32_3	H	level	X
14	~apxgpt_irq_b0[4]	GPT_32_4	H	level	X
15	~apxgpt_irq_b0[5]	GPT_64	H	level	X
16	~devapc_INFRA_AON_secure_vio_irq_b	devapc secure violate	H	level	X
17	~devapc_AUD_BUS_PDN_secure_vio_irq_b	AUDIO_BUS devapc secure violate	H	level	X
18	conn_ap_bus_req_rise_irq	conn_ap_bus_req rising edge IRQ	H	level	X
19	conn_ap_bus_req_fall_irq	conn_ap_bus_req falling edge IRQ	H	level	X
20	conn_apsrc_req_rise_irq	conn_apsrc_req rising edge IRQ	H	level	X
21	conn_apsrc_req_fall_irq	conn_apsrc_req falling edge IRQ	H	level	X
22	conn_ap_bus_req_high_irq	conn_ap_bus_req level high IRQ	H	level	X
23	conn_ap_bus_req_low_irq	conn_ap_bus_req level low IRQ	H	level	X
24	conn_apsrc_req_high_irq	conn_apsrc_req level high IRQ	H	level	X
25	conn_apsrc_req_low_irq	conn_apsrc_req level low IRQ	H	level	X
26	infra_bus_timeout_irq	infra bus timeout IRQ	H	level	X
27	cm33_local_bus_int	CM33 local bus interrupt	H	level	X
28	adsp_infra_bus_timeout_irq	dsp_infra bus timeout IRQ	H	level	X
29	Reserved				
30	Reserved				
31	Reserved				
32	~dsp_uart_irq_b	DSP UART	H	level	X
33	~top_uart0_irq_b	TOP UART	H	level	X

MCU IRQ NUM	Interrupt Name	Interrupt Description	Polarity	Edge / Level	EINT
34	~top_uart1_irq_b	TOP UART	H	level	X
35	~i2c0_irqb	I2C transfer done or error	H	level	X
36	~i2c1_irqb	I2C transfer done or error	H	level	X
37	~sdctl_top_fw_irq_b	SDIO slave interrupt	H	level	X
38	~sdctl_top_fw_irq_b_qout	SDIO slave interrupt	H	level	X
39	~spi_irq_b	SPI master transfer done or pause	H	level	X
40	~spi_irq_b	SPI master transfer done or pause	H	level	X
41	~spis_irq_b	SPI slave transfer done	H	level	X
42	~kp_irq_b	keypad key pressed scanning done	H	edge	X
43	~irrx_irq_b	IRRX decoding done	H	level	X
44	Reserved				
45	Reserved				
46	Reserved				
47	Reserved				
48	ssusb_xhci_int	USB xHCI event interrupt	H	level	X
49	ssusb_otg_int	USB OTG interrupt	H	level	X
50	ssusb_dev_int	USB device interrupt	H	level	X
51	~audio_irq_mcu_b	AFE interrupt	H	level	X
52	~rtc_irq_b	RTC interrupt	H	level	X
53	sysram_top_int	SYSRAM out-of-bound access error	H	level	X
54	~mpu_irq_b_l2_pwr	illegal accesses to asic_mpu instances in L2	H	level	X
55	~mpu_irq_b_psram_pwr	illegal accesses to asic_mpu for PSRAM	H	level	X
56	~cq_dma_irq_b[0]	CQ_DMA Channel 0 finishes operation	H	level	X
57	~cq_dma_irq_b[1]	CQ_DMA Channel 1 finishes operation	H	level	X
58	~cq_dma_irq_b[2]	CQ_DMA Channel 2 finishes operation	H	level	X
59	~msdc_irq_b_0p	normal IRQ	H	level	X
60	~msdc_wakeup_ps_0p	wakeup IRQ	H	level	X
61	~dspwdt_irq_b	DSP WDT IRQ	H	level	X
62	dsp2cpu_irq	DSP to CPU IRQ	H	level	X
63	~ap_dma_irq_b[0]	AP_DMA Channel 0 (I2C 0) finishes operation	H	level	X
64	~ap_dma_irq_b[1]	AP_DMA Channel 1 (I2C 1) finishes operation	H	level	X
65	~ap_dma_irq_b[2]	AP_DMA Channel 2 (Reserved) finishes operation	H	level	X
66	~ap_dma_irq_b[3]	AP_DMA Channel 3 (Reserved) finishes operation	H	level	X
67	~ap_dma_irq_b[4]	AP_DMA Channel 4 (UART 0 TX) finishes operation	H	level	X

MCU IRQ NUM	Interrupt Name	Interrupt Description	Polarity	Edge / Level	EINT
68	~ap_dma_irq_b[5]	AP_DMA Channel 5 (UART 0 RX) finishes operation	H	level	X
69	~ap_dma_irq_b[6]	AP_DMA Channel 6 (UART 1 TX) finishes operation	H	level	X
70	~ap_dma_irq_b[7]	AP_DMA Channel 7 (UART 1 RX) finishes operation	H	level	X
71	~ap_dma_irq_b[8]	AP_DMA Channel 8 (BTIF TX) finishes operation	H	level	X
72	~ap_dma_irq_b[9]	AP_DMA Channel 9 (BTIF RX) finishes operation	H	level	X
73	~ap_dma_irq_b[10]	AP_DMA Channel 10 (Reserved) finishes operation	H	level	X
74	~ap_dma_irq_b[11]	AP_DMA Channel 11 (AUXADC RX) finishes operation	H	level	X
75	~btif_host_irq_b	BTIF host interrupt	H	level	X
76	~flash_int_b	Flash Controller Interrupt	H	level	X
77	~conn2ap_wfdma_irq_b	Wi-Fi host interrupt	H	level	X
78	~bgf2ap_wdt_irq_b	bgf WDT interrupt	H	edge	X
79	~bgf2ap_btif0_wakeup_out_b	bgf BTIF wakeup interrupt	H	level	X
80	~conn2ap_sw_irq_b	bgf software interrupt for debug	H	level	X
81	~bt2ap_isoch_irq_b	bt iso channel interrupt	H	level	X
82	~bt_cvsd_int_b	bt CVSD interrupt	H	level	X
83	~ccif_wf2ap_sw_irq_b	wf software interrupt for debug from ccif trigger	H	level	X
84	~ccif_bgf2ap_sw_irq_b	bgf software interrupt for debug from ccif trigger	H	level	X
85	~wm_conn2ap_wdt_irq_b		H	edge	X
86	~sema_release_inform_m2_int_b	semaphore release IRQ for m2	H	level	X
87	~sema_release_inform_m3_int_b	semaphore release IRQ for m3	H	level	X
88	~sema_m2_timeout_int_b	semaphore timeout IRQ for m2	H	level	X
89	~sema_m3_timeout_int_b	semaphore timeout IRQ for m3	H	level	X
90	~conn_bgf_hif_on_host_int_b				
91	Reserved				
92	ssusb_spm_int	USB SPM wakeup IRQ	H	level	X
93	~wf2ap_sw_irq_b	wf2ap software IRQ	H	level	X
94	cq_dma_sec_abort	CQ_DMA APB secure violation happens	H	level	X
95	ap_dma_sec_abort	AP_DMA APB secure violation happens	H	level	X
96	~sdio_sdio_cmd_i	SDIO slave wakeup interrupt	H	edge	X
97	Reserved				
98	~adc_comp_irq_b	ADC comparator IRQ	H	level	X
99	~adc_fifo_int_b	ADC FIFO mode interrupt	H	level	X
100	~gcpu_irq_b	GCPU interrupt	H	level	X

MCU IRQ NUM	Interrupt Name	Interrupt Description	Polarity	Edge / Level	EINT
101	~ecc_irq_b	ECC interrupt	H	level	X
102	~trng_irq_b	TRNG interrupt	H	level	X
103	~sej_apxgpt_irq_b	SEJ GPT interrupt	H	level	X
104	~sej_wdt_irq_b	SEJ WDT interrupt	H	level	X
105	Reserved				
106	Reserved				
107	Reserved				
108	gpio_irq[0]	GPIO IRQ	H	configurable	V
109	gpio_irq[1] / sdio_sdio_cmd_i	GPIO IRQ / sdio_sdio_cmd_i	H	configurable	V
110	gpio_irq[2]	GPIO IRQ	H	configurable	V
111	gpio_irq[3]	GPIO IRQ	H	configurable	V
112	gpio_irq[4]	GPIO IRQ	H	configurable	V
113	gpio_irq[5]	GPIO IRQ	H	configurable	V
114	gpio_irq[6]	GPIO IRQ	H	configurable	V
115	gpio_irq[7]	GPIO IRQ	H	configurable	V
116	gpio_irq[8]	GPIO IRQ	H	configurable	V
117	gpio_irq[9]	GPIO IRQ	H	configurable	V
118	gpio_irq[10]	GPIO IRQ	H	configurable	V
119	gpio_irq[11]	GPIO IRQ	H	configurable	V
120	gpio_irq[12]	GPIO IRQ	H	configurable	V
121	gpio_irq[13]	GPIO IRQ	H	configurable	V
122	gpio_irq[14]	GPIO IRQ	H	configurable	V
123	gpio_irq[15]	GPIO IRQ	H	configurable	V
124	gpio_irq[16]	GPIO IRQ	H	configurable	V
125	gpio_irq[17]	GPIO IRQ	H	configurable	V
126	gpio_irq[18]	GPIO IRQ	H	configurable	V
127	gpio_irq[19]	GPIO IRQ	H	configurable	V
128	gpio_irq[20]	GPIO IRQ	H	configurable	V
129	gpio_irq[21]	GPIO IRQ	H	configurable	V
130	gpio_irq[22]	GPIO IRQ	H	configurable	V
131	gpio_irq[23]	GPIO IRQ	H	configurable	V
132	gpio_irq[24]	GPIO IRQ	H	configurable	V
133	gpio_irq[25]	GPIO IRQ	H	configurable	V
134	gpio_irq[26]	GPIO IRQ	H	configurable	V
135	gpio_irq[27]	GPIO IRQ	H	configurable	V
136	gpio_irq[28]	GPIO IRQ	H	configurable	V
137	gpio_irq[29]	GPIO IRQ	H	configurable	V
138	gpio_irq[30] / ~sdio_sdio_cmd_i	GPIO IRQ / ~sdio_sdio_cmd_i	H	configurable	V

MCU IRQ NUM	Interrupt Name	Interrupt Description	Polarity	Edge / Level	EINT
139	~cm33_pad_uart_rx / ~sdio_sdio_cmd_i	~cm33_pad_uart_rx / ~sdio_sdio_cmd_i	H	configurable	V

3 Radio Characteristics

3.1 Wi-Fi Radio Characteristics

3.1.1 Wi-Fi RF Block Diagram

Figure 3-1 illustrates the Wi-Fi RF function block. The MT7933CT integrates LNA, PA, and TRSW.
The frond-end loss with diplexer: The insertion loss for 2.4 GHz band is 1.5 dB, while the insertion loss for 5 GHz band is 2 dB.

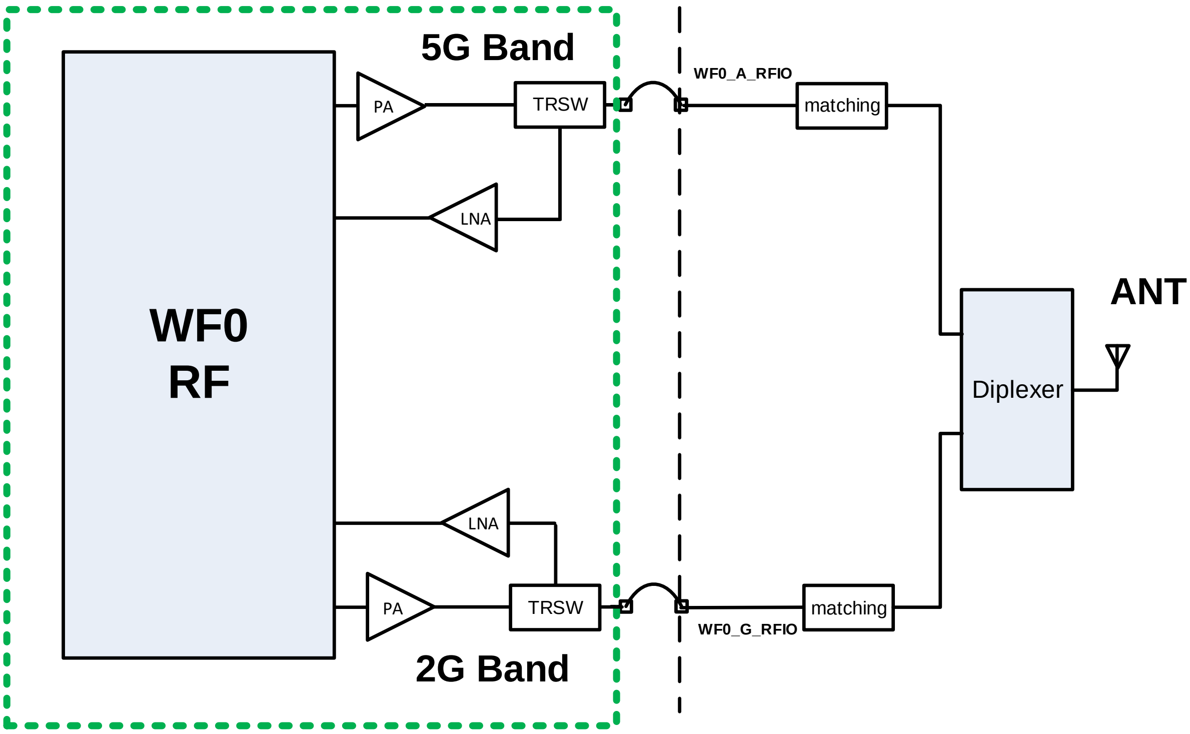


Figure 3-1 Wi-Fi RF block diagram

3.1.2 Wi-Fi RF 2.4G Band Receiver Specifications

The specifications listed in the table below are measured at the antenna port with the front-end loss.

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		2412	-	2484	MHz
RX sensitivity	1 Mbps CCK	-	-96.5	-	dBm
	2 Mbps CCK	-	-93	-	dBm
	5.5 Mbps CCK	-	-91	-	dBm
	11 Mbps CCK	-	-88	-	dBm
RX sensitivity	6 Mbps OFDM	-	-93.5	-	dBm
	9 Mbps OFDM	-	-91	-	dBm
	12 Mbps OFDM	-	-90.5	-	dBm
	18 Mbps OFDM	-	-88	-	dBm
	24 Mbps OFDM	-	-84.5	-	dBm
	36 Mbps OFDM	-	-81.5	-	dBm
	48 Mbps OFDM	-	-77	-	dBm
	54 Mbps OFDM	-	-75.5	-	dBm
RX Sensitivity BW=20 MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-92.5	-	dBm
	MCS 1	-	-89	-	dBm
	MCS 2	-	-87	-	dBm
	MCS 3	-	-84	-	dBm
	MCS 4	-	-80.5	-	dBm
	MCS 5	-	-76	-	dBm
	MCS 6	-	-75	-	dBm
	MCS 7	-	-73.5	-	dBm
RX Sensitivity VHT20 BCC	MCS 0		-92.5		dBm
	MCS 1		-89		dBm
	MCS 2		-87		dBm
	MCS 3		-84		dBm
	MCS 4		-80.5		dBm
	MCS 5		-76		dBm
	MCS 6		-75		dBm
	MCS 7		-73.5		dBm
	MCS 8		-69		dBm
RX Sensitivity HE20 BCC (4 x LTF)	MCS0	-	-92	-	dBm
	MCS1	-	-88.5	-	dBm
	MCS2	-	-86	-	dBm
	MCS3	-	-83	-	dBm
	MCS4	-	-80	-	dBm
	MCS5	-	-75.5	-	dBm
	MCS6	-	-74	-	dBm
	MCS7	-	-72.5	-	dBm
	MCS8	-	-68.5	-	dBm
Maximum Receive Level	11 Mbps CCK	-	-10	-	dBm
	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
Receive Adjacent Channel Rejection	1 Mbps CCK	-	43	-	dBm
	11 Mbps CCK	-	41	-	dBm
	6 Mbps OFDM	-	41	-	dBm
	54 Mbps OFDM	-	25	-	dBm
Receive Adjacent Channel Rejection (HT20)	MCS 0	-	36	-	dBm
	MCS 7	-	13	-	dBm

Sensitivity level at 25°C and 3.3V

3.1.3 Wi-Fi RF 2.4G Band Transmitter Specifications

The specifications in the table below are measured at the antenna port with the frond-end loss.

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		2412	-	2484	MHz
Output power at 25°C and 3.3V with mask and EVM compliance	1~11 Mbps CCK	-	21.5	-	dBm
	6 Mbps OFDM	-	20.5	-	dBm
	54 Mbps OFDM	-	18	-	dBm
	HT20, MCS 0	-	19.5	-	dBm
	HT20, MCS 7	-	17.5	-	dBm
	VHT20, MCS 0	-	19.5	-	dBm
	VHT20, MCS 8	-	16.5	-	dBm
	HE20, MCS 0	-	19.5	-	dBm
	HE20, MCS 8	-	16.5	-	dBm
Output power variation[1]	TSSI closed-loop control across all temperature range and channels and VSWR ≦ 1.5:1.	-2		2	dB
Carrier suppression		-		-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-	dBm/MHz
	3nd Harmonic	-	-45	-	dBm/MHz

Note 1: VDD33 is within ±5% of typical value

3.1.4 Wi-Fi RF 5G Band Receiver Specifications

The specifications listed in the table below are measured at the antenna port with the front-end loss.

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		5180	-	5825	MHz
RX sensitivity	6 Mbps OFDM	-	-93	-	dBm
	9 Mbps OFDM	-	-90.5	-	dBm
	12 Mbps OFDM	-	-90	-	dBm
	18 Mbps OFDM	-	-87.5	-	dBm
	24 Mbps OFDM	-	-84	-	dBm
	36 Mbps OFDM	-	-81	-	dBm
	48 Mbps OFDM	-	-76.5	-	dBm
	54 Mbps OFDM	-	-75	-	dBm
RX Sensitivity BW=20 MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-92	-	dBm
	MCS 1	-	-88.5	-	dBm
	MCS 2	-	-86.5	-	dBm
	MCS 3	-	-83.5	-	dBm
	MCS 4	-	-80	-	dBm
	MCS 5	-	-75.5	-	dBm
	MCS 6	-	-74.5	-	dBm
	MCS 7	-	-73	-	dBm
	MCS 8	-	-68.5	-	dBm
RX Sensitivity HE20 BCC (4 x LTF)	MCS 0	-	-91.5	-	dBm
	MCS 1	-	-88	-	dBm
	MCS 2	-	-85.5	-	dBm
	MCS 3	-	-82.5	-	dBm
	MCS 4	-	-79.5	-	dBm
	MCS 5	-	-75	-	dBm
	MCS 6	-	-73.5	-	dBm
	MCS 7	-	-72	-	dBm
	MCS 8	-	-68	-	dBm
Maximum Receive Level	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
Receive Adjacent Channel Rejection (VHT20)	MCS0	-	27	-	dBm
	MCS8	-	0	-	dBm

Sensitivity level at 25°C and 3.3V

3.1.5 Wi-Fi RF 5G Band Transmitter Specifications

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		5180	-	5825	MHz
Output power at 25℃ and 3.3V with mask and EVM compliance	6 Mbps OFDM	-	21	-	dBm
	54 Mbps OFDM	-	18.5	-	dBm
	HT20, MCS 0	-	20	-	dBm
	HT20, MCS 7	-	17.5	-	dBm
	HE20, MCS8	-	16.5	-	dBm
Output power variation[1]	TSSI closed-loop control across all temperature range and channels and VSWR ≦1.5:1.	-2		2	dB
Carrier suppression		-		-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-	dBm/MHz
	3nd Harmonic	-	-45	-	dBm/MHz

3.2 Bluetooth Radio Characteristics

3.2.1 Bluetooth RF Block Diagram

Figure 3-2 illustrates the Bluetooth RF function block. The MT7933CT integrates LNA, PA, and TRSW. The frond-end losses are both 0.2 dB.

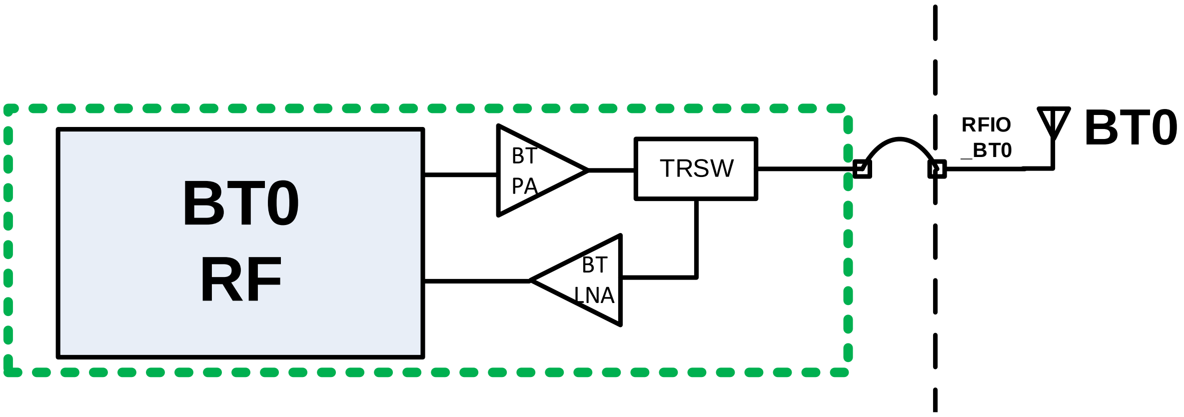


Figure 3-2 Bluetooth RF block diagram

3.2.2 Basic Rate Receiver Specifications

The specifications listed in the table below are measured at the antenna port with the front-end loss.

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		2402	-	2480	MHz
Receiver sensitivity[1]	BER<0.1%	-	-94.5	-70	dBm
Maximum usable signal	BER<0.1%	-20	-	-	dBm
C/I co-channel (BER<0.1%)	Co channel selectivity	-	6	11	dB
C/I 1 MHz (BER<0.1%)	Adjacent channel selectivity	-	-6	0	dB
C/I 2 MHz (BER<0.1%)	2nd adjacent channel selectivity	-	-40	-30	dB
C/I ≥ 3 MHz (BER<0.1%)	3rd adjacent channel selectivity	-	-43	-40	dB
C/I Image channel (BER<0.1%)	Image channel selectivity	-	-20	-9	dB
C/I Image 1MHz (BER<0.1%)	1 MHz adjacent to image channel selectivity	-	-35	-20	dB
Inter-modulation		-39	-30	-	dBm
Out-of-band blocking	30 MHz to 2000 MHz	-10	-	-	dBm
	2000 MHz to 2399 MHz	-27	-	-	dBm
	2498 MHz to 3000 MHz	-27	-	-	dBm
	3000 MHz to 12.75 GHz	-10	-	-	dBm

Note 1: The receiver sensitivity is measured at the antenna port.

3.2.3 Basic Rate Transmitter Specifications

The specifications listed in the table below are measured at the antenna port with the front-end loss.

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		2402	-	2480	MHz
Output power[1]	At maximum power output level	-	14.5	-	dBm
Gain step		2	5	8	dB
Modulation characteristics	Δf1avg	140	157	175	kHz
	Δf2max (For at least 99.9% of all Δf2max)	115	145	-	kHz
	Δf1avg /Δf2avg	0.8	0.9	-	kHz
ICFT	Initial carrier frequency tolerance	-75	±18	+75	kHz
Carrier frequency drift	One slot packet (DH1)	-25	±10	+25	kHz
	Two slot packets (DH3)	-40	±10	+40	kHz
	Five slot packets (DH5)	-40	±10	+40	kHz
	Max drift rate	-	10	20	kHz/50µs
TX output spectrum	20-dB bandwidth	-	922	1000	kHz
In-Band spurious emission	± 2 MHz offset	-	-38	-20	dBm
	± 3 MHz offset	-	-43	-40	dBm
	>± 3 MHz offset	-	-45	-40	dBm

Note 1: The output power is measured at the antenna port.

3.2.4 Enhanced Data Rate Receiver Specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		2402	-	2480	MHz
Receiver sensitivity (BER<0.01%)[1]	π/4 DQPSK	-	-94	-	dBm
	8PSK	-	-87	-	dBm
Maximum usable signal (BER<0.1%)	π/4 DQPSK	-20	-	-	dBm
	8PSK	-20	-	-	dBm
C/I co-channel (BER<0.1%)	π/4 DQPSK	-	9	13	dB
	8PSK	-	16	21	dB
C/I 1 MHz (BER<0.1%)	π/4 DQPSK	-	-11	0	dB
	8PSK	-	-5	5	dB
C/I 2 MHz (BER<0.1%)	π/4 DQPSK	-	-40	-30	dB
	8PSK	-	-29	-25	dB
C/I ≥ 3 MHz (BER<0.1%)	π/4 DQPSK	-	-43	-40	dB
	8PSK	-	-40	-33	dB
C/I Image channel (BER<0.1%)	π/4 DQPSK	-	-20	-7	dB
	8PSK	-	-15	0	dB
C/I Image 1 MHz (BER<0.1%)	π/4 DQPSK	-	-40	-20	dB
	8PSK	-	-30	-13	dB

Note 1: The receiver sensitivity is measured at the antenna port.

3.2.5 Enhanced Data Rate Transmitter Specifications

The specifications in table below are measured at the antenna port with the frond-end loss.

Parameter	Description		Performance Min.	Typ.	Max.	Unit
Maximum transmit power[1]	π/4 DQPSK		-	11.5	-	dBm
	8PSK		-	11.5	-	dBm
Relative transmit power	π/4 DQPSK		-	-3	-	dB
	8PSK		-	-3	-	dB
Frequency stability	maximum carrier frequency stability, ωo	π/4 DQPSK	-10	±4	10	kHz
		8PSK	-10	±4	10	kHz
	maximum carrier frequency stability, ωi	π/4 DQPSK	-75	±18	75	kHz
		8PSK	-75	±18	75	kHz
	maximum carrier frequency stability, |ωo + ωi|	π/4 DQPSK	-75	±20	75	kHz
		8PSK	-75	±20	75	kHz
Modulation accuracy	RMS DEVM	π/4 DQPSK	-	8	20	%
		8PSK	-	8	13	%
	99% DEVM	π/4 DQPSK	-	11	-	%
		8PSK	-	11	-	%
	Peak DEVM	π/4 DQPSK	-	15	35	%
		8PSK	-	15	25	%
In-Band spurious emission	± 1 MHz offset	π/4 DQPSK	-	-29	-26	dB
	± 1 MHz offset	8PSK	-	-29	-26	dB
	± 2 MHz offset	π/4 DQPSK	-	-23	-20	dBm
	± 2 MHz offset	8PSK	-	-23	-20	dBm
	± 3 MHz offset	π/4 DQPSK	-	-40	-40	dBm
	± 3 MHz offset	8PSK	-	-40	-40	dBm

Note 1: The output power is measured at the antenna port.

3.2.6 Bluetooth LE Un-coded PHY Receiver Specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Min.	Typ.	Max.	Unit
Channel Frequency Coverage		2402	-	2480	MHz
Receiver Sensitivity (*)	BLE 1Mbps(PER < 30.8%)	-	-97	-	dBm
	BLE 2Mbps(PER < 30.8%)	-	-94	-	
Max. Usable Signal	BLE 1Mbps(PER < 30.8%)	-10	-	-	dBm
	BLE 2Mbps(PER < 30.8%)	-10	-	-	dBm
C/I Co-channel	BLE 1Mbps(PER < 30.8%)	-	9	21	dB
C/I 1MHz		-	-3	15	dB
C/I 2MHz		-	-30	-17	dB
C/I ≧3MHz		-	-33	-27	dB
C/I Image channel		-	-20	-9	dB
C/I Image 1MHz		-	-30	-15	dB
C/I Co-channel	BLE 2Mbps(PER < 30.8%)	-	7	21	dB
C/I 1MHz		-	-3	15	dB
C/I 2MHz		-	-27	-17	dB
C/I ≧3MHz		-	-30	-27	dB
C/I Image channel		-	-17	-9	dB
C/I Image 1MHz		-	-27	-15	dB
Out-of-band Blocking	30MHz to 2000MHz	-30	-	-	dBm
	2001MHz to 2339MHz	-35	-	-	dBm
	2501MHz to 3000MHz	-35	-	-	dBm
	3001MHz to 12.75GHz	-30	-	-	dBm

Note 1: The receiver sensitivity is measured at the BT antenna port.

3.2.7 Bluetooth LE Un-Coded PHY Transmitter Specifications

The specifications in table below are measured at the antenna port with the frond-end loss.

Parameter	Description		Min.	Typ.	Max.	Unit
Channel frequency coverage			2402	-	2480	MHz
Output Power (*)	BLE 1Mbps		-	14.5	-	dBm
	BLE 2Mbps		-	14.5	-	
Carrier Frequency Offset and Drift	Frequency offset	BLE 1Mbps	-150	±10	150	kHz
		BLE 2Mbps	-150	±10	150	
	Frequency drift	BLE 1Mbps	-50	±10	50	kHz
		BLE 2Mbps	-50	±10	50	
	Max. drift rate	BLE 1Mbps	-20	±10	20	KHz/50us
		BLE 2Mbps	-20	±10	20	
Modulation Characteristic	$\Delta f1_{avg}$	BLE 1Mbps	225	250	275	kHz
		BLE 2Mbps	450	500	550	
	$\Delta f2_{max}$ (For at least 99% of all $\Delta f2_{max}$)	BLE 1Mbps	185	-	-	kHz
		BLE 2Mbps	370	-	-	
	$\Delta f2_{avg}/\Delta f1_{avg}$	BLE 1Mbps	0.8	0.9	-	
		BLE 2Mbps	0.8	0.9	-	
In-band Spurious Emission	±2MHz offset	BLE 1Mbps	-	-35	-20	dBm
	±4MHz,±5MHz offset	BLE 2Mbps	-	-35	-20	
	>±3MHz offset	BLE 1Mbps	-	-40	-30	dBm

Note 1: The output power is measured at the antenna port.

3.2.8 Bluetooth LE Coded PHY Receiver Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
Channel frequency coverage		2402	-	2480	MHz
Receiver sensitivity (*)	BLE 500Kbps (PER < 30.8%)	-	-98	-	dBm
	BLE 125Kbps (PER < 30.8%)	-	-103	-	
C/I co-channel	BLE 500Kbps (PER < 30.8%)	-	5	17	dB
	BLE 125Kbps (PER < 30.8%)	-	6	12	
C/I 1MHz	BLE 500Kbps (PER < 30.8%)	-	-8	11	dB

Parameter	Description	Min.	Typ.	Max.	Unit
	BLE 125Kbps (PER < 30.8%)	-	-12	6	
C/I 2MHz	BLE 500Kbps (PER < 30.8%)	-	-34	-21	dB
	BLE 125Kbps (PER < 30.8%)	-	-39	-26	
C/I ≧3MHz	BLE 500Kbps (PER < 30.8%)	-	-37	-31	dB
	BLE 125Kbps (PER < 30.8%)	-	-42	-36	
C/I image channel	BLE 500Kbps (PER < 30.8%)	-	-24	-13	dB
	BLE 125Kbps (PER < 30.8%)	-	-29	-18	
C/I Image 1MHz	BLE 500Kbps (PER < 30.8%)	-	-34	-19	dB
	BLE 125Kbps (PER < 30.8%)	-	-39	-24	

Note 1: The receiver sensitivity is measured at the BT antenna port.

3.2.9 Bluetooth LE Coded PHY Transmitter Specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description		Min.	Typ.	Max.	Unit
Channel frequency coverage			2402	-	2480	MHz
Output power(*)	BLE 500Kbps		-	14.5	-	dBm
	BLE 125Kbps		-	14.5	-	
Carrier frequency offset and drift	Frequency offset	BLE 125Kbps	-150	±10	150	kHz
	Frequency drift	BLE 125Kbps	-50	±10	50	kHz
	Max. drift rate	BLE 125Kbps	-19.2	±10	19.2	KHz/48us
Modulation characteristic	$\triangle f1_{avg}$	BLE 125Kbps	225	250	275	kHz
	△f1max (For at least 99% of all △f1max)	BLE 125Kbps	185	245	-	kHz

Note 1: The output power is measured at the BT antenna port.

4 Electrical Characteristics

4.1 Absolute Maximum Rating

Table 4-1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.63	V
AVDD33_RTC	RTC Supply Voltage	-0.3 to 4.2	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	1000	V

4.2 Recommended Operating Range

Table 4-2 Recommended operating range

Symbol	Rating	Min.	Typ.	Max.	Unit
VDD33	3.3V Supply Voltage	2.97	3.3	3.63	V
AVDD33_RTC	RTC Supply Voltage	2.5		4.2	V
$T_{JUNCTION}$	Junction Temperature	-30	-	125	°C

4.3 DC Characteristics

Table 4-3 DC characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage	LVTTL	-0.3	0.25*VDD33	V
V_{IH}	Input High Voltage		0.625*VDD33	VDD33+0.3	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 2~8 mA	-0.3	0.45	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 2~8 mA	VDD33-0.45	VDD33+0.3	V
R_{PU0}	Input Pull-Up Resistance	PUPD=low, R0=high, R1=low	5	10	kΩ
R_{PD0}	Input Pull-Down Resistance	PUPD=high, R0=high, R1=low	5	10	kΩ
R_{PU1}	Input Pull-Up Resistance	PUPD=low, R0=low, R1=high	10	100	kΩ
R_{PD1}	Input Pull-Down Resistance	PUPD=high, R0=low, R1=high	10	100	kΩ

4.4 XTAL Oscillator

The table below lists the requirement for the XTAL.

Table 4-4 XTAL oscillator requirement

Parameter	Value
Frequency	26 MHz
Frequency stability over operating temperature range	±10 ppm (referred to the value at 25°C)
Aging	±3 ppm/year

4.5 PMU Characteristics

Table 4-5 PMU electrical characteristics

PARAMETER	CONDITIONS	PERFORMANCE			
		Min.	Typ.	Max.	UNIT
BUCK-R (Switching regulator)					
Input voltage		2.97	3.3	3.63	V
Output voltage		1.14	1.2	1.32	V
Output current		-	-	550	mA
Quiescent current		-	150	180	uA
Efficiency	100~200 mA load current	84	87	-	%
Over-current Shutdown		1	1.3	1.6	A
BUCK-D (Switching regulator)					
Input voltage		2.97	3.3	3.63	V
Output voltage		0.62	0.7	0.85	V
Output current		-	-	1400	mA
Quiescent current		-	150	180	uA
Efficiency	10~200 mA load current	79	82	-	%
Over-current Shutdown		1.3	1.7	2.1	A
PHYLDO					
Input voltage		2.97	3.3	3.63	V
Output voltage		1.62	1.8	1.98	V
Output current		-	-	150	mA
Quiescent current		-	10	20	uA
ALDO					
Input voltage		2.97	3.3	3.63	V

PARAMETER	CONDITIONS	PERFORMANCE			
		Min.	Typ.	Max.	UNIT
Output voltage		1.62	1.8	1.98	V
Output current		-	-	150	mA
Quiescent current		-	10	20	uA
AUXLDO					
Input voltage		2.97	3.3	3.63	V
Output voltage		1.62	1.8	1.98	V
Output current		-	-	1	mA
Quiescent current		-	10	20	uA
MLDO					
Input voltage		1.14	1.2	1.26	V
Output voltage		0.62	0.8	0.88	V
Output current		-	-	120	mA
Quiescent current		-	10	20	uA
General					
AVDD33 UVLO rising threshold		-	2.85	-	V
AVDD33 UVLO falling threshold		-	2.7	-	V
PMU_EN high threshold		1.09	1.2	1.31	V
PMU_EN low threshold		0.8	0.9	1	V
Thermal shutdown			150		°C

4.6 Auxiliary ADC Characteristics

This section specifies the electrical characteristics of the auxiliary ADC.

Table 4-6 ADC specification

Symbol	Parameter	Min.	Typ.	Max.	Unit	
N	Resolution		12		Bit	
CH	Channel Number		12		Channel	12 AGPIOs in digital part
FC	Clock Rate	1	2	6	MHz	
FS	Sampling Rate @ N-Bit	1	2	6	MSPS	FS = 2 MHz by default
TS	Sample period	0.17	0.5	1	µS	= 1/FS
VPP	Input Swing			1	V	
VIN	Input voltage	0		1	V	
SC	Sampling capacitance		2.048		pF	

Symbol	Parameter	Min.	Typ.	Max.	Unit	
RIN	Series Input Impedance: Unselected channel Selected channel			400M 10K	Ohm	
	Dither waveform type		Sawtooth			
	Dither step size (programmable)	0	4	4	LSB	Programmable (0,4)
N_{avg}	Number of samples averaged in hardware (programmable)	1	32	64		Programmable (1, 2, 4, 8, 16, 32, 64)
T_{dither}	Dither period	1	16	16	TS	Programmable(1, 2, 4, 8, 16)
	Dither Magnitude	0	64	64	LSB	= DITHERSTEP*T_{dither}
DNL	Differential Nonlinearity without dithering and averaging		± 1	± 2	LSB	No dither and no averaging
INL	Integral Nonlinearity without dithering and averaging		± 2	± 4	LSB	
$DNL_{dither+average}$	Differential Nonlinearity with dithering and averaging		± 0.5	± 1	LSB	With dither and averaging
$INL_{dither+average}$	Integral Nonlinearity with dithering and averaging			± 4	LSB	
OE	Offset Error			± 10	mV	
FSE	Full Swing Error			± 50	mV	
SNR	Signal to Noise Ratio	55	58	61	dB	@ 1 kHz input frequency
DVDD	Digital Power Supply	0.54	0.8	0.88	V	Have VAD Mode
AVDD	Analog Power Supply	1.62	1.8	1.98	V	
IOVDD	IO Power Supply	1.62	1.8	1.98	V	
T	Operating Temperature	-40		125	℃	
	Current Consumption			400	µA	
	Power-Down Current			1	µA	

4.7 Audio DAC

This section specifies the electrical characteristics of the Audio DAC.

Table 4-7 DAC specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
	3.3V Analog Power(V33)	3.135	3.3	3.465	V
	Digital Power Supply(V10)	0.585	0.8	0.88	V
AUDIO Down-Link: Fully-Differential LO Amplifier fully-differential output					
	Clock Frequency (FCK)		6.5		MHz
	Sample Rate (Fs)	32	44.1	48	kHz
	Current Consumption (IDC)		6.5		mA
	Peak Signal to Noise Ratio (PSNR)；A-weighting		105		dB
	Dynamic Range (DR)；A-weighting @-60dBFS Input		105		dB
	Output Swing for 0dBFS Input Level			1	Vrms
	Total Harmonic Distortion Plus Noise (THD+N) @Rload=10 kΩ; A-weighting		-90		dB
	Output Resistor Load(Differential)	5	10		kΩ
	L-R Channel Crosstalk(XT)	80	100		dB

4.8 Audio ADC

This section specifies the electrical characteristics of the Audio ADC.

Table 4-8 ADC specification

Symbol	Parameter	Min.	Typ.	Max.	Unit
	3.3V Analog Power(V33)	3.135	3.3	3.465	V
	Digital Power Supply(V10)	0.585	0.8	0.88	V
AUDIO Up-Link: Fully-Differential					
	Clock Frequency (FCK)		26		MHz
	Current Consumption (IDC)		4		mA
	Signal to Noise Ratio (SNR) ; A-weighting		90		dB
	Dynamic Range (DR) ; A-weighting @-60dBFS Input		90		dB
	Input Swing @ PGA Gain 0 dB		0.7		Vrms
	Total Harmonic Distortion Plus Noise (THD+N); A-weighting		-83		dB
	Input PGA Gain Step		2		dB
	Input PGA Gain	-6	0	24	dB
	L-R Channel Crosstalk (XT)		95		dB
	Input Impedance	13	20	27	kΩ
	MICBIAS Voltage	1.9		2.2	V

4.9 Thermal Characteristics

Θ_{JC} assumes that all the heat is dissipated through the top of the package, while Ψ_{Jt} assumes that the heat is dissipated through the top, sides, and the bottom of the package. Thus it's suggested to use Ψ_{Jt} to estimate the junction temperature.

Symbol	Description	Performance	
		Typical	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance	33.53	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	10.74	°C/W
Ψ_{Jt}	Junction to the package thermal resistance	2.24	°C/W

Note: JEDEC 51-9 system FR4 PCB size: 101.5x114.5mm (4"x4.5"), 2 layer.

Table 4-9-1 Thermal characteristics

Symbol	Description	Performance	
		Typical	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C

Θ_{JA}	Junction to ambient temperature thermal resistance	24.28	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	10.74	°C/W
Ψ_{Jt}	Junction to the package thermal resistance	1.94	°C/W

Note: JEDEC 51-9 system FR4 PCB size: 101.5x114.5mm (4”x4.5”), 4 layer.

Table 4-9-2 Thermal characteristics

5 Package Specification

5.1 Pin Layout

The MT7933CT uses the BGA package of 21x21 ball array with 10.6mm x 10.6mm dimension and 0.5mm ball pitch.

284	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	
A	NC	AVDD33_WF0_G_TX	WF0_G_RFIO	GND_RF	GND_RF	AVDD33_WF0_A_PA	WF0_A_RFIO	AVDD33_WF0_A_TX	AVDD18_WF0_TRX	AVDD33_RTC		CVCC_T		VCCIO_T		AVDD33_BT		AVDD18_BT	AVDD12_BT	GPIO_R_11	NC	A
B	AVDD12_WF0_TRX	GND_RF	GND_RF	GND_RF	AVDD33_WF0_G_PA	GND_RF	GND_RF	GND_RF	GND_RF	AVSS_RTC		VCC18_T	GPIO_T_8	GPIO_T_4	GPIO_T_2		RFIO_BT	GND_RF		GPIO_R_9	GPIO_R_7	B
C	AVDD18_WF0_TOP	GND_RF	GND_RF					WF0_RFDET		XIN	XOUT		GPIO_T_10	GPIO_T_6	GPIO_T_0	GND_RF		GND_RF	GPIO_R_6	GPIO_R_2	GPIO_R_4	C
D	WF0_SX_MON		GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF			GPIO_T_9		GPIO_T_3		GND_RF		GPIO_R_8	GPIO_R_0	GPIO_R_5	GPIO_R_1	D
E	AVDD12_WF0_AFE	GND_RF	GND_RF	GND_RF		GND_RF			GND_RF		DVDD_RTC	GPIO_T_11		GPIO_T_7		GND_RF		GPIO_R_10	VCC18_PSRAM	GPIO_R_3		E
F	AVDD12_XO	GND_RF		GND_RF	GND_RF		GND_RF	GND_RF	GND_RF		IO18PWR_RTC	RTC_PMU_EN		GPIO_T_5				VCC18_PSRAM	VCCIO_R	CVCC_R	AVDD33_AUDIO	F
G		GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	GND_RF	RTC_EVT			GPIO_T_1		GND_RF				AVSS33_AUDIO	VMID	G
H	GND_RF	XO_IP	XO_IN		GND_RF		DVSS	DVSS	DVSS	DVSS	DVSS	DVDD	DVDD	DVDD	DVDD	DVSS	VCC18_R		AU_VOLN	AU_VOLP		H
J				GND_RF	GND_RF	GND_RF		DVSS		DVSS		DVSS		DVDD	DVDD	DVDD			AU_REFN			J
K	AVDD18_PLL	AVSS18_PLL	TP_PLL0	TN_PLL0	GND_RF	GND_RF	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD	DVDD			AU_VORP	AU_VORN		K
L	AVDD18_USB	AVDD33_USB		AVSS18_PLL				DVSS		DVSS		DVSS		DVDD		DVDD			AVSS33_AUDIO	AU_TP	AU_TN	L
M		AVSS33_USB			AVDD18_PLL		DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVSS	DVDD				AU0_VIN0_P	AU0_VIN0_N			M
N	USB_DM	USB_DP		USB_VBUS	DVDD	DVDD	DVDD	DVSS		DVSS		DVSS		DVDD					AVSS33_AUDIO	AU0_VIN1_P	AU0_VIN1_N	N
P	DVSS		SF_QPI_D0			DVDD	DVDD	DVDD					DVDD	DVDD				MICBIAS0				P
R	SF_QPI_D3	SF_QPI_CS	SF_QPI_D1					DVDD	DVDD	DVDD			AVSS33_MISC_BUCKD	AVSS33_ESD_BUCKD			DVSS		AU1_VIN0_N	AU1_VIN0_P		R
T		SF_QPI_D2	SF_QPI_CK	CVCC_L	VCCIO_L	VCC18_L	DVSS		AVDD18_AUXADC		DVDD	DVDD		AVSS33_ESD_BUCKR	AVSS33_MISC_BUCKR					AVSS33_AUDIO	MICBIAS1	T
U		SDIO_CMD	SDIO_DAT1	SDIO_DAT2	VCC18_L				AVSS18_AUXADC			DVDD				PMU_AT	VO_FB_BUCKD	VO_FB_BUCKR			VREF_PMU	U
V	SDIO_DAT0		SDIO_CLK	SDIO_DAT3			GPIO_B_10		AUXIN0	EMI_TN									AVDD33		PHYLDO18	V
W	GPIO_B_1	SYSRST_B	GPIO_B_0	GPIO_B_2	GPIO_B_4	GPIO_B_9	GPIO_B_14		VREF_DDR	EMI_EXTR	AVDDQ_EMI	AVDDQ_EMI							AVSS33		ALDO18	W
Y	GPIO_B_3	GPIO_B_5	GPIO_B_7	GPIO_B_6	GPIO_B_11	GPIO_B_13	GPIO_B_15		AVDD18_RDDR	AVDD18_RDDR	AVDDQ_EMI	DVSS	AVDD33_BUCKD	AVSS33_BUCKD	LX_BUCKD				AVSS33_MISC2	PMU_EN	AUXLDO18	Y
AA	NC	VCCIO_B	GPIO_B_8		GPIO_B_12		GPIO_B_16	CVCC_B		DVSS	AVDDQ_EMI	DVSS	AVDD33_BUCKD	AVSS33_BUCKD	LX_BUCKD	LX_BUCKR	AVSS33_BUCKR	AVDD33_BUCKR	MLDO_VOUT	AVDD12	NC	AA
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	

Figure 5-1 Package ball-out

5.2 Pin Description

The section describes pin functionalities of the MT7933CT chip.

Table 5-1 Pin descriptions

BGA	Pin Name	Pin description
WF RF		
E1	AVDD12_WF0_AFE	RF 1.2V power supply
B1	AVDD12_WF0_SX_HF	RF 1.2V power supply
F1	AVDD12_XO	RF 1.2V power supply
C1	AVDD18_WF_TOP	RF 1.8V power supply
A9	AVDD18_WF0_A_TRX	RF 1.8V power supply
A6	AVDD33_WF0_A_PA	RF 3.3V power supply
A8	AVDD33_WF0_A_TX	RF 3.3V power supply
B5	AVDD33_WF0_G_PA	RF 3.3V power supply
A2	AVDD33_WF0_G_TX	RF 3.3V power supply
B2/B3/B4/B6/B7/B8/B9/B18/C2/C3/C16/C18/D3/D4/D5/D6/D7/D8/D9/D16/E2/E3/E4/E6/E9/E16/F2/F4/F5/F7/F8/F9/G2/G3/G4/G5/G6/G7/G8/G9/G10/G16/H1/H5/J4/J5/J6/K5/K6	AVSS_WF_LF	RF ground
A7	WF0_A_RFIO	RF a-band RF port
A3	WF0_G_RFIO	RF g-band RF port
C8	WF0_RFDET	Detection port for external PA output voltage
A5	WF0_RXA_AUX_IN	RF a-band auxiliary RF LNA port
A4	WF0_RXG_AUX_IN	RF a-band auxiliary RF LNA port
H3	XO_IN	Crystal input
H2	XO_IP	Crystal input or external clock input
D1	XO_MON	Clock monitor for debug purpose
PLL		
K1/M5	AVDD18_PLLGP	PLL 1.8V power
K2/L4	AVSS18_PLLGP	PLL ground
K4	TN_TOPPLL	Performance testing
K3	TP_TOPPLL	Performance testing
USB		
L1	AVDD18_USB	USB20 1.8V
L2	AVDD33_USB	USB20 3.3V

BGA	Pin Name	Pin description
M2	AVSS33_USB	Ground
N1	USB_DM	USB20 D- Signal 480Mbps
N2	USB_DP	USB20 D+ Signal 480Mbps
N4	USB_VBUS	USB20 VBUS
AUXADC		
T9	AVDD18_VREF18_AUXADC	AUXADC 1.8V power
U9	AVSS18_AUXADC	AUXADC ground
V9	AUXIN0	AUXADC analog test input pin
PSRAM		
W11/W12/Y11/AA11	AVDDQ_EMI	PSRAM 1.2V power
Y9/Y10	AVDD18_RDDR	PSRAM 1.8V power
W10	EMI_EXTR	External Resistor for Calibration
V10	EMI_TN	Test pin
W9	VREF_DDR	Reference voltage for DDR
PMU		
AA20	AVDD12	MLDO 1.2V supply
Y13/AA13	AVDD33_BUCKD	BUCKD 3.3V supply
AA18	AVDD33_BUCKR	BUCKR 3.3V supply
V19	AVDD33	PMU 3.3V supply
Y14/AA14	AVSS33_BUCKD	BUCKD power stage ground
AA17	AVSS33_BUCKR	BUCKR power stage ground
R14	AVSS33_ESD_BUCKD	BUCKD power stage substrate ground
T14	AVSS33_ESD_BUCKR	BUCKR power stage substrate ground
W19	AVSS33	PMU ground
R13	AVSS33_MISC_BUCKD	BUCKD controller GND
T15	AVSS33_MISC_BUCKR	BUCKR controller GND
Y19	AVSS33_MISC2	PMU ground
W21	ALDO18	ALDO 1.8V output pin
Y21	AUXLDO18_S	AUXLDO 1.8V output pin
Y15/AA15	LX_BUCKD	BUCKD switch node
AA16	LX_BUCKR	BUCKR switch node
AA19	MLDO_VOUT	MLDO 0.8V output pin
V21	PHYLDO18	PHYLDO 1.8V output pin
U16	PMU_AT	PMU analog test pin
Y20	PMU_EN	PMU enable signal

BGA	Pin Name	Pin description
U17	VO_FB_BUCKD	BUCKD output voltage feedback signal
U18	VO_FB_BUCKR	BUCKR output voltage feedback signal
U21	VREF_PMU	1.2V reference voltage
CODEC		
F21	AVDD33_AUDIO	Audio Codec 3.3V power
G20/L19/N19/T20	AVSS33_AUDIO	Audio Codec ground
N21	AU0_VIN1_N	CODEC_ADC ADC0 RCH N_port input
N20	AU0_VIN1_P	CODEC_ADC ADC0 RCH P_port input
P18	MICBIAS0	CODEC_ADC ADC0 MICBIAS output
M19	AU0_VIN0_N	CODEC_ADC ADC0 LCH N_port input
M18	AU0_VIN0_P	CODEC_ADC ADC0 LCH P_port input
T21	MICBIAS1	CODEC_ADC ADC1 MICBIAS output
L21	AU_TN	CODEC_ADC Test_N point
L20	AU_TP	CODEC_ADC Test_P point
R19	AU1_VIN0_N	CODEC_ADC ADC1 LCH N_port input
R20	AU1_VIN0_P	CODEC_ADC ADC1 LCH P_port input
J19	AU_REFN	CODEC clean ground
H19	AU_VOLN	CODEC_DAC Left_channel N_port output signal
H20	AU_VOLP	CODEC_DAC Left_channel P_port output signal
K20	AU_VORN	CODEC_DAC Right_channel N_port output signal
K19	AU_VORP	CODEC_DAC Right_channel P_port output signal
G21	VMID	CODEC_DAC reference voltage
BT RF		
A19	AVDD12_TSSI_ADC_BT	BT 1.2V power
A18	AVDD18_BT	BT 1.8V power

BGA	Pin Name	Pin description
A16	AVDD33_BT	BT 3.3V power
B17	RFIO_BT	RF BT RF port
RTC		
A10	AVDD33_RTC	RTC Supply Voltage
B10	AVSS_RTC	RTC ground
C10	XIN	Crystal input Pin
C11	XOUT	Crystal input Pin
F11	IO18PWR_RTC	IO 1.8V power
E11	DVDD_RTC	External DVDD source for RTC domain
G11	RTC_EVT	External wakeup from RTC mode Max. 1.8V
F12	PMU_EN	External power supply enable output
PSRAM (DIG)		
E19/F18	VCC18_PSRAM	PSRAM 1.8V power
Digital Power		
A12/F20/T4/AA8	CVCC_T/CVCC_R/CVCC_L/CVCC_B	Memory power
H12/H13/H14/H15/J14/J15/J16/K15/K16/L14/L16/M14/N5/N6/N7/N14/P6/P7/P8/P13/P14/R8/R9/R10/T11/T12/U12	DVDD	Digital core power
T6	VCC18_L	Digital IO 1.8V power
U5	VCC18_L	Digital IO 1.8V power
H17	VCC18_R	Digital IO 1.8V power
B12	VCC18_T	Digital IO 1.8V power
AA2	VCCIO_B	Digital IO power
T5	VCCIO_L	Digital IO power
F19	VCCIO_R	Digital IO power
A14	VCCIO_T	Digital IO power
H7/H8/H9/H10/H11/H16/J8/J10/J12/K7/K8/K9/K10/K11/K12/K13/K14/L8/L10/L12/M7/M8/M9/M10/M11/M12/M13/N8/N10/N12/P1/R17/T7/Y12/AA10/AA12	DVSS	Digital ground
RESET and GPIO		
W3	GPIO_B_0	GPIO
W1	GPIO_B_1	GPIO

BGA	Pin Name	Pin description
W4	GPIO_B_2	GPIO
Y1	GPIO_B_3	GPIO
W5	GPIO_B_4	GPIO
Y2	GPIO_B_5	GPIO with AUXADC Channel Interface
Y4	GPIO_B_6	GPIO with AUXADC Channel Interface
Y3	GPIO_B_7	GPIO with AUXADC Channel Interface
AA3	GPIO_B_8	GPIO with AUXADC Channel Interface
W6	GPIO_B_9	GPIO with AUXADC Channel Interface
V7	GPIO_B_10	GPIO with AUXADC Channel Interface
Y5	GPIO_B_11	GPIO with AUXADC Channel Interface
AA5	GPIO_B_12	GPIO with AUXADC Channel Interface
Y6	GPIO_B_13	GPIO with AUXADC Channel Interface
W7	GPIO_B_14	GPIO with AUXADC Channel Interface
Y7	GPIO_B_15	GPIO with AUXADC Channel Interface
AA7	GPIO_B_16	GPIO with AUXADC Channel Interface
D19	GPIO_R_0	GPIO
D21	GPIO_R_1	GPIO
C20	GPIO_R_2	GPIO
E20	GPIO_R_3	GPIO
C21	GPIO_R_4	GPIO
D20	GPIO_R_5	GPIO
C19	GPIO_R_6	GPIO
B21	GPIO_R_7	GPIO
D18	GPIO_R_8	GPIO
B20	GPIO_R_9	GPIO
E18	GPIO_R_10	GPIO
A20	GPIO_R_11	GPIO

BGA	Pin Name	Pin description
C15	GPIO_T_0	GPIO
G14	GPIO_T_1	GPIO
B15	GPIO_T_2	GPIO
D14	GPIO_T_3	GPIO
B14	GPIO_T_4	GPIO
F14	GPIO_T_5	GPIO
D12	KPCOL_0	GPIO with Keypad Interface
C13	KPCOL_1	GPIO with Keypad Interface
E12	KPCOL_2	GPIO with Keypad Interface
C14	KPROW_0	GPIO with Keypad Interface
E14	KPROW_1	GPIO with Keypad Interface
B13	KPROW_2	GPIO with Keypad Interface
V3	SDIO_CLK	GPIO with SDIO Interface
U2	SDIO_CMD	GPIO with SDIO Interface
V1	SDIO_DAT0	GPIO with SDIO Interface
U3	SDIO_DAT1	GPIO with SDIO Interface
U4	SDIO_DAT2	GPIO with SDIO Interface
V4	SDIO_DAT3	GPIO with SDIO Interface
T3	SF_QPI_CK	Flash Interface
R2	SF_QPI_CS	Flash Interface
P3	SF_QPI_D0	Flash Interface
R3	SF_QPI_D1	Flash Interface
T2	SF_QPI_D2	Flash Interface
R1	SF_QPI_D3	Flash Interface
W2	SYSRST_B	Chip hardware fundamental reset pin
A1	NC	Unused pins
A21	NC	Unused pins
AA1	NC	Unused pins
AA21	NC	Unused pins

5.3 PinMux

The pin multiplexing can be controlled via the table shown below.

Table 5-2 Digital IO pin configuration in each pad and the corresponding pin description

IO Name	CR Value Default*	Name	Dir	Default Dir	Default PU/PD	Description
PAD_SYSRST_B	NA	PAD_SYSRST_B			PU	Chip hardware fundamental reset pin
SDIO_CLK	0000	GPIO[6]	I/O	I	PD	GPIO 6
	0001 *	SDIO_CLK	I			SDIO Clock
	0010	MSDC0_CLK	O			MSDC Clock
	0011	SPIM0_SCK	O			SPI0 (Master) Clock
	0100	CM33_GPIO_EINT0	I			CM33 EINT0
	0101	DEBUG_0	O			Debug Signal 0
	0110	ANT_SEL0	O			Antenna Select 0
	0111	RSVD	I			RSVD
SDIO_CMD	0000	GPIO[7]	I/O	I	PU	GPIO 7
	0001 *	SDIO_CMD	I/O			SDIO CMD
	0010	MSDC0_CMD	I/O			MSDC CMD
	0011	SPIM0_CS_N	O			SPI0 (Master) Chip Select
	0100	CM33_GPIO_EINT1	I			CM33 EINT1
	0101	DEBUG_1	O			Debug Signal 1
	0110	ANT_SEL1	O			Antenna Select 1
	0111	RSVD	I			RSVD
SDIO_DAT0	0000	GPIO[8]	I/O	I	PU	GPIO 8
	0001 *	SDIO_DAT0	O			SDIO Data[0]
	0010	MSDC0_DAT0	I/O			MSDC0 Data[0]
	0011	SPIM0_MISO	I			SPI0 (Master) Input
	0100	UART0_RTS	O			UART0 RTS
	0101	DEBUG_2	O			Debug Signal 2
	0110	ANT_SEL2	O			Antenna Select 2
	0111	CM33_GPIO_EINT0	I			CM33 EINT0
SDIO_DAT1	0000	GPIO[9]	I/O	I	PU	GPIO 9
	0001 *	SDIO_DAT1	I/O			SDIO Data[1]
	0010	MSDC0_DAT1	I/O			MSDC0 Data[1]
	0011	SPIM0_MOSI	O			SPI0 (Master) Output
	0100	UART0_CTS	I			UART0 CTS
	0101	DEBUG_3	O			Debug Signal 3
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CM33 EINT1
SDIO_DAT2	0000	GPIO[10]	I/O	I	PU	GPIO 10
	0001 *	SDIO_DAT2	I/O			SDIO Data[2]
	0010	MSDC0_DAT2	I/O			MSDC0 Data[2]
	0011	I2SIN_DAT0	I			I2S In Data0
	0100	UART0_RX	I			UART0 RX
	0101	DEBUG_4	O			Debug Signal 4
	0110	I2C0_SCL	O			I2C0 Clock
	0111	CM33_GPIO_EINT2	I			CM33 EINT2
SDIO_DAT3	0000	GPIO[11]	I/O	I	PU	GPIO 11

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0001 *	SDIO_DAT3	I/O			SDIO Data[3]
	0010	MSDC0_DAT3	I/O			MSDC Data[3]
	0011	I2SO_DAT0	O			I2SO Data
	0100	UART0_TX	O			UART0 TX
	0101	DEBUG_5	O			Debug Signal 5
	0110	I2C0_SDA	I/O			I2C0 Data
	0111	CM33_GPIO_EINT3	I			CM33 EINT3
GPIO_B_0	0000	GPIO[12]	I/O	O	PU	GPIO 12
	0001 *	CONN_BGF_UART0_TXD	O			BT General UART TX
	0010	MSDC0_RST	O			MSDC0 Reset
	0011	CONN_BT_TXD	O			BT Debug UART TX
	0100	WIFI_TXD	O			Wi-Fi Debug UART TX
	0101	DEBUG_6	O			Debug Signal 6
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT4	I			CM33 EINT4
GPIO_B_1	0000	GPIO[13]	I/O	I	PU	GPIO 13
	0001 *	USB_IDDIG	I			USB OTG ID Pin
	0010	SPIM1_SCK	O			SPIM1 (Master) Clock
	0011	I2SO_BCK	O			I2SO BCK
	0100	UART1_RX	I			UART1 RX
	0101	DEBUG_7	O			Debug Signal 7
	0110	ANT_SEL4	O			Antenna Select 4
	0111	CM33_GPIO_EINT5	I			CM33 EINT5
GPIO_B_2	0000	GPIO[14]	I/O	O	PD	GPIO 14
	0001 *	USB_DRV_VBUS	O			USB OTG VBUS
	0010	SPIM1_MOSI	O			SPI1 (Master) Output
	0011	I2SO_LRCK	O			I2SO LRCK
	0100	RSVD				RSVD
	0101	DEBUG_8	O			Debug Signal 8
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT6	I			CM33 EINT6
GPIO_B_3	0000	GPIO[15]	I/O	I	PD	GPIO 15
	0001 *	USB_OC	I			USB Host Mode Over-Current Input Notify
	0010	SPIM1_MISO	I			SPI1 (Master) Input
	0011	I2SO_MCK	O			I2STX MCLK
	0100	I2SIN_MCK	O			I2SRX MCK
	0101	DEBUG_9	O			Debug Signal 9
	0110	ANT_SEL6	O			Antenna Select 6
	0111	CM33_GPIO_EINT7	I			CM33 EINT7
GPIO_B_4	0000	GPIO[16]	I/O	I	PD	GPIO 16
	0001 *	USB_VBUS_VALID	I			USB Device Mode VBUS Detect
	0010	SPIM1_CS_N	O			SPI1 (Master) Chip Select
	0011	IR_IN	I			IR RX Input
	0100	I2SIN_MCK	O			I2SIN MCLK
	0101	DEBUG_10	O			Debug Signal 10
	0110	ANT_SEL7	O			Antenna Select 7

IO Name	CR Value Default*	Name	Dir	Default Dir	Default PU/PD	Description
	0111	CM33_GPIO_EINT8	I			CM33 EINT8
GPIO_B_5	0000	GPIO[17]	I/O	I	PU	GPIO 17
	0001 *	CONN_BGF_UART0_RXD	I			BT General UART RX
	0010	UART0_RX	I			UART0 RX
	0011	TDMIN_MCLK	I			TDMIN MCLK
	0100	DMIC_CLK0	O			DMIC CLK0
	0101	DEBUG_11	O			Debug Signal 11
	0110	ANT_SEL8	O			Antenna Select 8
	0111	CM33_GPIO_EINT9	I			CM33 EINT9
GPIO_B_6	0000	GPIO[18]	I/O	O	PU	GPIO 18
	0001 *	CONN_BT_TXD	O			BT Debug UART TX
	0010	UART0_TX	O			UART0 TX
	0011	TDMIN_BCK	I			TDMIN BCK
	0100	DMIC_DAT0	I			DMIC DAT0
	0101	UART1_RX	I			UART1 RX
	0110	IR_IN	I			IR RX Input
	0111	CM33_GPIO_EINT10	I			CM33 EINT10
GPIO_B_7	0000	GPIO[19]	I/O	O	PD	GPIO 19
	0001 *	WIFI_TXD	O			Wi-Fi Debug UART TX
	0010	UART0_RTS	O			UART0 RTS
	0011	I2C1_SDA	I/O			I2C1 Data
	0100	I2SIN_LRCK	O			I2SIN LRCK
	0101	UART1_TX	O			UART1 TX
	0110	PTA_EXT_IF_FREQ	I			External PTA Frequency
	0111	CM33_GPIO_EINT11	I			CM33 EINT11
GPIO_B_8	0000	GPIO[20]	I/O	I	PD	GPIO 20
	0001 *	CONN_WF_MCU_AICE_TCKC	I			Wi-Fi N10 SWD
	0010	UART0_CTS	I			UART0 Control
	0011	I2C1_SCL	O			I2C1 Clock
	0100	I2SIN_BCK	O			I2SIN BCK
	0101	DEBUG_12	O			Debug Signal 12
	0110	PTA_EXT_IF_ACT	I			External PTA Active
	0111	CM33_GPIO_EINT12	I			CM33 EINT12
GPIO_B_9	0000	GPIO[21]	I/O	I	PU	GPIO 21
	0001 *	CONN_WF_MCU_AICE_TMSC	I/O			Wi-Fi N10 SWD
	0010	PTA_EXT_IF_PRI	I/O			External PTA Priority
	0011	TDMIN_LRCK	I/O			TDMIN LRCK
	0100	DMIC_DAT1	I			DMIC DAT1
	0101	DEBUG_13	O			Debug Signal 13
	0110	ANT_SEL9	O			Antenna Select 9
	0111	CM33_GPIO_EINT13	I			CM33 EINT13
GPIO_B_10	0000	GPIO[22]	I/O	I	PD	GPIO 22
	0001 *	CONN_BGF_MCU_AICE_TCKC	I			BT N10 SWD
	0010	PTA_EXT_IF_WLAN_ACT	O			External PTA WLAN Active
	0011	TDMIN_DI	I			TDMIN DI
	0100	DMIC_DAT2	I			DMIC Data2
	0101	DEBUG_14	O			Debug Signal 14
	0110	ANT_SEL10	O			Antenna Select 10

IO Name	CR Value Default*	Name	Dir	Default Dir	Default PU/PD	Description
	0111	CM33_GPIO_EINT14	I			CM33 EINT14
GPIO_B_11	0000	GPIO[23]	I/O	I	PU	GPIO 23
	0001 *	CONN_BGF_MCU_AICE_TMSC	I/O			BT N10 SWD
	0010	DSP_URXD0	I			DSP UART RX
	0011	I2C0_SDA	I/O			I2C0 Data
	0100	DMIC_DAT3	I			DMIC Data3
	0101	DEBUG_15	O			Debug Signal 15
	0110	ANT_SEL11	O			Antenna Select 11
	0111	CM33_GPIO_EINT15	I			CM33 EINT15
GPIO_B_12	0000	GPIO[24]	I/O	O	PU	GPIO 24
	0001 *	ADSP_JTAG_TDO	O			DSP JTAG
	0010	DSP_UTXD0	O			DSP UART TX
	0011	I2C0_SCL	O			I2C0 Clock
	0100	DMIC_CLK1	O			DMIC CLK1
	0101	RSVD	O			RSVD
	0110	ANT_SEL12	O			Antenna Select 12
	0111	CM33_GPIO_EINT16	I			CM33 EINT16
GPIO_B_13	0000	GPIO[25]	I/O	I	PD	GPIO 25
	0001 *	ADSP_JTAG_TCK	I			DSP JTAG
	0010	RSVD	I			RSVD
	0011	UART0_RX	I			UART0 RX
	0100	SPIM0_SCK	O			SPIM0 Clock
	0101	RSVD				RSVD
	0110	UART1_RX	I			UART1 RX
	0111	SPIS_SCK	I			SPIS_SCK
GPIO_B_14	0000	GPIO[26]	I/O	I	PU	GPIO 26
	0001 *	ADSP_JTAG_TRST	I			DSP JTAG
	0010	CM33_UART_TX	O			CM33 UART TX
	0011	UART0_TX	O			UART0 TX
	0100	SPIM0_CS_N	O			SPIM0 CS
	0101	RSVD				RSVD
	0110	UART1_TX	O			UART1 TX
	0111	SPIS_CS_N	I			SPIS_CS_N
GPIO_B_15	0000	GPIO[27]	I/O	I	PU	GPIO 27
	0001 *	ADSP_JTAG_TDI	I			DSP JTAG
	0010	RSVD	O			RSVD
	0011	UART0_RTS	O			UART0 RTS
	0100	SPIM0_MISO	I			SPIM0 MISO
	0101	RSVD				RSVD
	0110	UART1_RTS	O			UART1 RTS
	0111	SPIS_MOSI	I			SPIS_MOSI
GPIO_B_16	0000	GPIO[28]	I/O	I	PU	GPIO 28
	0001 *	ADSP_JTAG_TMS	I			DSP JTAG
	0010	RSVD	I			RSVD
	0011	UART0_CTS	I			UART0 CTS
	0100	SPIM0_MOSI	O			SPIM0 MOSI
	0101	SPIS_MISO	O			SPIS MISO
	0110	UART1_CTS	I			UART1 CTS

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0111	CM33_GPIO_EINT20	I			CM33_GPIO_EINT20
GPIO_R_0	0000	GPIO[29]	I/O	I	PU	GPIO29
	0001 *	DSP_URXD0	I			DSP UART RX
	0010	ADSP_JTAG_TDO	O			DSP JTAG
	0011	PWM_0	O			PWM0
	0100	PTA_EXT_IF_PRI	I/O			External PTA Priority
	0101	CONN_WF_MCU_TDO	O			Wi-Fi N10 JTAG
	0110	RSVD	I			RSVD
	0111	CM33_GPIO_EINT21	I			CM33 EINT21
GPIO_R_1	0000	GPIO[30]	I/O	O	PD	GPIO 30
	0001 *	DSP_UTXD0	O			DSP UART TX
	0010	ADSP_JTAG_TCK	I			DSP JTAG
	0011	PWM_1	O			PWM 1
	0100	PTA_EXT_IF_WLAN_ACT	O			External PTA WLAN Active
	0101	CONN_WF_MCU_TCK	I			Wi-Fi N10 JTAG
	0110	CM33_RSVD3	I/O			RSVD
	0111	CM33_GPIO_EINT22	I			CM33 EINT22
GPIO_R_2	0000	GPIO[31]	I/O	O	PD	GPIO 31
	0001 *	USB_DRV_VBUS	O			USB Host mode VBUS driving
	0010	ADSP_JTAG_TRST	I			DSP JTAG
	0011	PWM_2	O			PWM2
	0100	PTA_EXT_IF_FREQ	I			External PTA Frequency
	0101	CONN_WF_MCU_TDI	I			Wi-Fi N10 JTAG
	0110	CM33_RSVD0	I			RSVD
	0111	CM33_GPIO_EINT23	I			CM33 EINT23
GPIO_R_3	0000	GPIO[32]	I/O	I	PD	GPIO 32
	0001 *	USB_OC	I			USB Host Mode Over-Current Input Notify
	0010	ADSP_JTAG_TDI	I			DSP JTAG
	0011	PWM_3	O			PWM 3
	0100	PTA_EXT_IF_ACT	I			External PTA Active
	0101	CONN_WF_MCU_TRSR_B	I			Wi-Fi N10 JTAG
	0110	RSVD	I			RSVD
	0111	CM33_GPIO_EINT24	I			CM33 EINT24
GPIO_R_4	0000	GPIO[33]	I/O	I	PD	GPIO 33
	0001 *	USB_VBUS_VALID	I			USB Device Mode VBUS Detect
	0010	ADSP_JTAG_TMS	I			DSP JTAG
	0011	PWM_4	O			PWM 4
	0100	I2C1_SDA	I/O			I2C1 Data
	0101	CONN_WF_MCU_TMS	I			Wi-Fi N10 JTAG
	0110	RSVD	O			RSVD
	0111	CM33_GPIO_EINT25	I			CM33 EINT25
GPIO_R_5	0000	GPIO[34]	I/O	I	PU	GPIO 34
	0001 *	USB_IDDIG	I			USB OTG ID Pin
	0010	I2C0_SCL	O			I2C0 Clock
	0011	PWM_5	O			PWM 5
	0100	I2C1_SCL	O			I2C1 Clock
	0101	RSVD	I			RSVD

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0110	DEBUG_0	O			Debug Signal 0
	0111	CM33_GPIO_EINT26	I			CM33 EINT26
GPIO_R_6	0000	GPIO[35]	I/O	O	PD	GPIO 35
	0001 *	UART0_TX	O			UART0 TX
	0010	RSVD	O			RSVD
	0011	PWM_6	O			PWM 6
	0100	PWM_2	O			PWM 2
	0101	CONN_BGF_MCU_TDO	O			BT N10 JTAG
	0110	DEBUG_1	O			Debug Signal 1
	0111	CM33_GPIO_EINT27	I			CM33 EINT27
GPIO_R_7	0000 *	GPIO[36]	I/O	I	PD	GPIO 36
	0001	DBSYS_NTRST	I			CM33 JTAG
	0010	CM33_UART_CTS	I			CM33 UART CTS
	0011	PWM_7	O			PWM 7
	0100	PWM_3	O			PWM 3
	0101	CONN_BGF_MCU_TCK	I			BT N10 JTAG
	0110	DEBUG_2	O			Debug Signal 2
	0111	CM33_GPIO_EINT28	I			CM33 EINT28
GPIO_R_8	0000 *	GPIO[37]	I/O	I	PD	GPIO 37
	0001	DBSYS_SWCLK_TCLK	I			CM33 JTAG
	0010	I2C1_SDA	I/O			I2C1 Data
	0011	PWM_8	O			PWM 8
	0100	I2C0_SDA	I/O			I2C0 Data
	0101	CONN_BGF_MCU_TDI	I			BT N10 JTAG
	0110	DEBUG_3	O			Debug Signal 3
	0111	CM33_GPIO_EINT29	I			CM33 EINT29
GPIO_R_9	0000 *	GPIO[38]	I/O	I	PD	GPIO 38
	0001	DBSYS_TDI	I			CM33 JTAG
	0010	CM33_UART_TX	O			CM33 UART TX
	0011	PWM_9	O			PWM 9
	0100	I2C0_SDA	I/O			I2C0 Data
	0101	CONN_BGF_MCU_TRST_B	I			BT N10 JTAG
	0110	I2C1_SCL	O			I2C1 Clock
	0111	CM33_GPIO_EINT30	I			CM33 EINT30
GPIO_R_10	0000 *	GPIO[39]	I/O	I	PD	GPIO 39
	0001	DBSYS_SWDIO_TMS	I/O			CM33 JTAG
	0010	I2C0_SDA	I/O			I2C0 Data
	0011	PWM_10	O			PWM 10
	0100	DSP_URXD0	I			DSP UART RX
	0101	CONN_BGF_MCU_TMS	I			BT N10 JTAG
	0110	ANT_SEL0	O			Antenna Select 0
	0111	RSVD	I			RSVD
GPIO_R_11	0000 *	GPIO[40]	I/O	O	PU	GPIO 40
	0001	DBSYS_TDO	O			CM33 JTAG
	0010	RSVD	I			RSVD
	0011	PWM_11	O			PWM 11
	0100	DSP_UTXD0	O			DSP UART TX
	0101	UART0_RX	I			UART0 RX

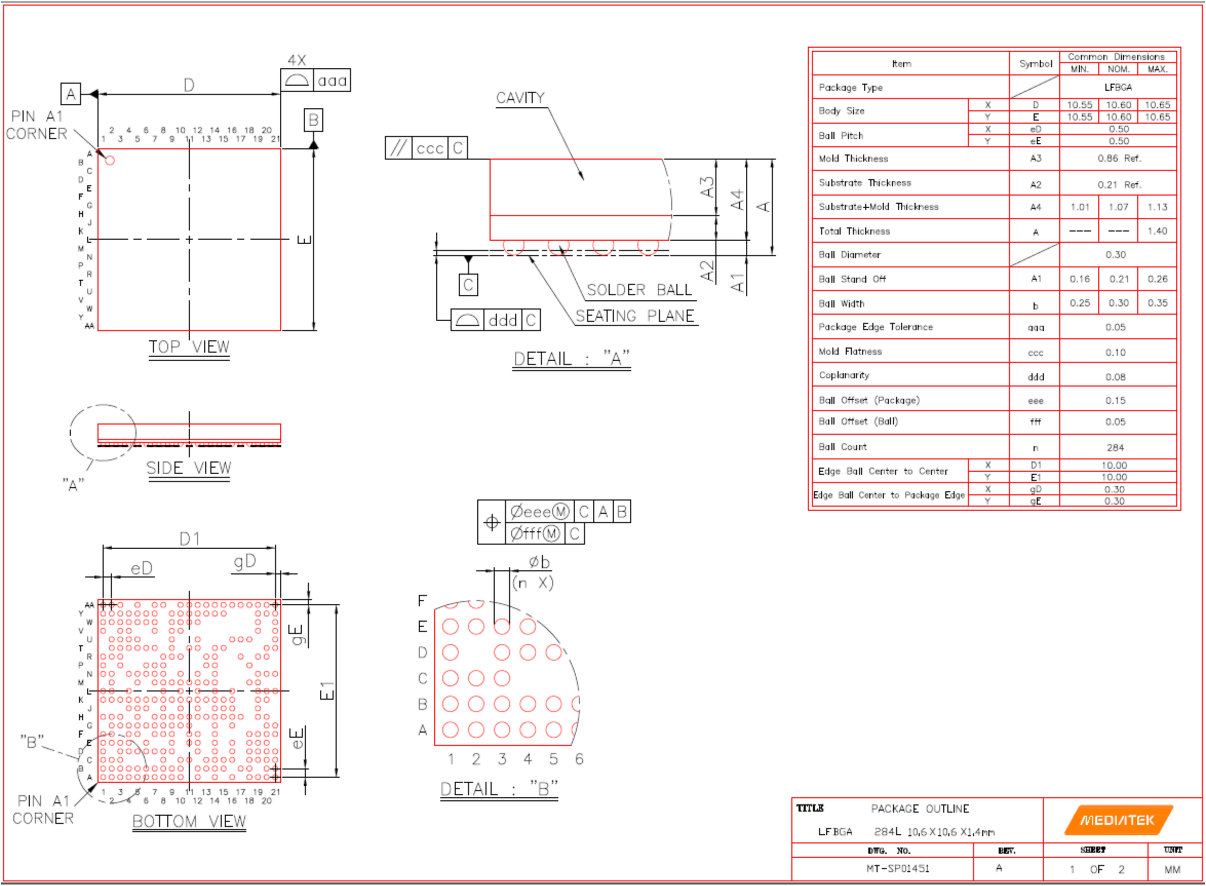
IO Name	CR Value Default*	Name	Dir	Default Dir	Default PU/PD	Description
	0110	ANT_SEL1	O			Antenna Select 1
	0111	RSVD	I			RSVD
GPIO_T_0	0000	GPIO[41]	I/O	I	PD	GPIO 41
	0001	RSVD	I			RSVD
	0010 *	DBSYS_NTRST	I			CM33 JTAG
	0011	I2C0_SDA	I/O			I2C0 Data
	0100	CONN_BGF_UART0_RXD	I			BT UART RX
	0101	I2C1_SDA	I/O			I2C1 Data
	0110	ANT_SEL2	O			Antenna Select 2
	0111	CM33_GPIO_EINT0	I			CM33 EINT0
GPIO_T_1	0000	GPIO[42]	I/O	I	PD	GPIO 42
	0001	RSVD	I			RSVD
	0010 *	DBSYS_SWCLK_TCLK	I			CM33_SWD (Default)
	0011	UART1_RX	I			UART1 RX
	0100	UART0_RX	I			UART0 RX
	0101	DSP_URXD0	I			DSP UART RX
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CM33 EINT1
GPIO_T_2	0000	GPIO[43]	I/O	I	PD	GPIO 43
	0001	RSVD	I			RSVD
	0010 *	DBSYS_TDI	I			CM33 JTAG
	0011	I2C0_SCL	O			I2C0 Clock
	0100	CONN_BGF_UART0_TXD	O			BT UART TX
	0101	I2C1_SCL	O			I2C1 Clock
	0110	ANT_SEL4	O			Antenna Select 4
	0111	CM33_GPIO_EINT17	I			CM33 EINT17
GPIO_T_3	0000	GPIO[44]	I/O	I	PD	GPIO 44
	0001	RSVD	I/O			RSVD
	0010 *	DBSYS_SWDIO_TMS	I			CM33_SWD (Default)
	0011	UART1_TX	O			UART1 TX
	0100	UART0_TX	O			UART0 TX
	0101	DSP_UTXD0	O			DSP UART TX
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT18	I			CM33 EINT18
GPIO_T_4	0000	GPIO[45]	I/O	O	PU	GPIO 45
	0001	RSVD	O			RSVD
	0010 *	DBSYS_TDOO	O			CM33 JTAG
	0011	I2C1_SDA	I/O			I2C1 Data
	0100	WIFI_TXD	O			Wi-Fi Debug UART TX
	0101	PWM_0	O			PWM0
	0110	ANT_SEL6	O			Antenna Select 6
	0111	CM33_GPIO_EINT19	I			CM33 EINT19
GPIO_T_5	0000	GPIO[46]	I/O	O	PU	GPIO 46
	0001 *	SPIM0_SCK	O			SPIM0 SCK
	0010	RSVD	O			RSVD
	0011	I2C1_SCL	O			I2C1 Clock
	0100	CONN_WF_MCU_AICE_TCKC	I			Wi-Fi N10 SWD
	0101	PWM_1	O			PWM 1

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0110	ANT_SEL7	O			Antenna Select 7
	0111	RSVD				RSVD
KPROW_0	0000	GPIO[47]	I/O	O	PU	GPIO 47
	0001 *	SPIM0_CS_N	O			SPIM0 CS
	0010	RSVD	O			RSVD
	0011	KEYPAD_KPROW_0	I/O			KEYPAD_KPROW_0
	0100	CONN_WF_MCU_AICE_TMSC	I/O			Wi-Fi N10 SWD
	0101	PWM_2	O			PWM 2
	0110	ANT_SEL8	O			Antenna Select 8
	0111	CM33_GPIO_EINT2	I			CM33 EINT2
KPROW_1	0000	GPIO[48]	I/O	I	PU	GPIO 48
	0001 *	CM33_UART_RX	I			CM33 UART RX (default)
	0010	RSVD	O			RSVD
	0011	KEYPAD_KPROW_1	I/O			KEYPAD_KPROW_1
	0100	DSP_URXD0	I			DSP UART RX
	0101	PWM_3	O			PWM 3
	0110	ANT_SEL9	O			Antenna Select 9
	0111	AUDIO_DEBUG_IN_0	I			AUDIO_DEBUG_IN_0
KPROW_2	0000	GPIO[49]	I/O	O	PU	GPIO 49
	0001 *	RSVD	O			RSVD
	0010	RSVD	O			RSVD
	0011	KEYPAD_KPROW_2	I/O			KEYPAD_KPROW_2
	0100	CONN_BT_TXD	O			BT Debug UART TX
	0101	PWM_4	O			PWM 4
	0110	ANT_SEL10	O			Antenna Select 10
	0111	AUDIO_DEBUG_IN_1	I			AUDIO_DEBUG_IN_1
KPCOL_0	0000	GPIO[50]	I/O	O	PU	GPIO 50
	0001 *	CM33_UART_TX	O			CM33 UART TX (default)
	0010	RSVD	O			RSVD
	0011	KEYPAD_KPCOL_0	I			KEYPAD_KPCOL_0
	0100	DSP_UTXD0	O			DSP UART TX
	0101	PWM_5	O			PWM 5
	0110	ANT_SEL11	O			Antenna Select 11
	0111	AUDIO_DEBUG_IN_2	I			AUDIO_DEBUG_IN_2
KPCOL_1	0000	GPIO[51]	I/O	I	PD	GPIO 51
	0001 *	SPIM0_MISO	I			SPIM0 MISO
	0010	RSVD	O			RSVD
	0011	KEYPAD_KPCOL_1	I			KEYPAD_KPCOL_1
	0100	CONN_BGF_MCU_AICE_TCKC	I			BT N10 SWD
	0101	PWM_6	O			PWM 6
	0110	ANT_SEL12	O			Antenna Select 12
	0111	AUDIO_DEBUG_IN_3	I			AUDIO_DEBUG_IN_3
KPCOL_2	0000	GPIO[52]	I/O	O	PU	GPIO 52
	0001 *	SPIM0_MOSI	O			SPIM0 MOSI
	0010	CM33_UART_RX	I			CM33 UART RX
	0011	KEYPAD_KPCOL_2	I			KEYPAD_KPCOL_2
	0100	CONN_BGF_MCU_AICE_TCKC	I/O			BT N10 SWD
	0101	PWM_7	O			PWM 7

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0110	UART1_TX	O			UART1 TX
	0111	AUDIO_DEBUG_IN_4	I			AUDIO_DEBUG_IN_4

5.5 Package Information

The MT7933CT uses the BGA 10.6mmx10.6mm package and the package diagram is shown below.



Item		Symbol	Common Dimensions MIN.	NOM.	MAX.
Package Type				LFBGA	
Body Size	X	D	10.55	10.60	10.65
	Y	E	10.55	10.60	10.65
Ball Pitch	X	eD		0.50	
	Y	eE		0.50	
Mold Thickness		A3		0.86 Ref.	
Substrate Thickness		A2		0.21 Ref.	
Substrate+Mold Thickness		A4	1.01	1.07	1.13
Total Thickness		A	---	---	1.40
Ball Diameter				0.30	
Ball Stand Off		A1	0.16	0.21	0.26
Ball Width		b	0.25	0.30	0.35
Package Edge Tolerance		aaa		0.05	
Mold Flatness		ccc		0.10	
Coplanarity		ddd		0.08	
Ball Offset (Package)		eee		0.15	
Ball Offset (Ball)		fff		0.05	
Ball Count		n		284	
Edge Ball Center to Center	X	D1		10.00	
	Y	E1		10.00	
Edge Ball Center to Package Edge	X	gD		0.30	
	Y	gE		0.30	

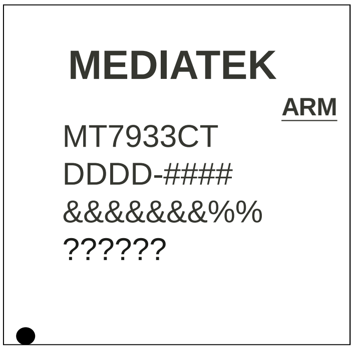
Figure 5-2 Package outline drawing

5.6 Order Information

Table 5-3 Order information

Part Number	Package
MT7933CT	10.6mm x 10.6mm x 1.4mm BGA284

5.7 Top Marking



->MT7933CT: Part number
->DDDD: Date code   ####: Internal control code
->&&&&&&&: Main die Lot Number %%: Main die wafer ID
->??????: KGD lot ID

Figure 5-3 Top marking

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