MT7931AN Datasheet

802.11a/b/g/n/ac/ax Wi-Fi 1T1R + Bluetooth 5.0 + ARM® Cortex®-M33

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0.1	2020-08-14	MediaTek	Initial draft
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1.1	2022-11-25	MediaTek	1. All content is same as v1.0, only update MediaTek document secure label

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0 Features

Wi-Fi

- IEEE 802.11 1T1R a/b/g/n/ac/ax 5 GHz and 2.4 GHz bands
- Supports 1x1 20 MHz bandwidth, MCS0~8(256-QAM) in 2.4/5 GHz band
- Support MU-MIMO RX
- Support uplink MU-OFDMA TX and downlink MU-OFDMA RX
- Support Tx LDPC(Low-density parity check)
- Support Rx Beamformee
- Support RX STBC
- Wi-Fi security WFA WPA/WPA2/WPA3 personal
- QoS support of WFA WMM
- Integrated balun, PA, LNA, and T/R switch
- Support CSI (Channel Signal Information)
- Supports antenna diversity
- Optional external LNA and PA support

Bluetooth

- BT5.0 2M_PHY / Long Range / Advertising Extension / SAM / CS#2 / High Duty Cycle Non-Connectable ADV
- BT4.2 Link Layer Privacy / LE Secure Connection / LE Data Packet Length Extension / Link Layer Extended Scanner Filter Policies
- BT4.1 Link Layer Topology / Secure Connection
- BT4.0 BLE only mode
- Integrated balun and PA
- Up to 8 BLE links
- Packet loss concealment
- Channel quality driven data rate adaptation
- Channel assessment and WB RSSI for AFH

Microcontroller Subsystem

- ARM® Cortex®-M33 with floating point unit (FPU) with 300MHz clock rate
- Supports 12 DMA channels
- Embedded 4MB pSRAM for applications
- Supports external serial flash with Quad Peripheral Interface (QPI) mode
- Supports eXecute In Place (XIP) on flash
- Supports interfaces: SDIO, SPI master, I2C, I2S, IR input, UART, AUXADC, PWM, and GPIOs
-

Secure Boot and Crypto Engine

- Secure boot from serial flash
- Hardware crypto engines including AES, DES/3DES, and SHA

Clock Source

- 26-MHz crystal oscillator
- 32-kHz external or internal crystal oscillator

Miscellaneous

- Advanced TDD Wi-Fi/Bluetooth coexistence scheme

1 System Overview

1.1 General Description

The MT7931AN is a highly integrated single chip that features an ARM® Cortex-M33 application processor, a low power 1x1 802.11a/b/g/n/ac/ax dual-band Wi-Fi subsystem, a Bluetooth v5.0 subsystem and a Power Management Unit (PMU). The Wi-Fi subsystem and a Bluetooth v5.0 subsystem offer feature-rich wireless connectivity at high standards, and deliver reliable, cost-effective throughput from an extended distance. Optimized RF architecture and baseband algorithms provide superb performance and low power consumption. The MT7931AN is designed to support standard based features in the areas of security, quality of service and international regulations, giving end users the greatest performance any time and in any circumstance.
The MT7931AN is based on ARM® Cortex-M33 with floating point microcontroller (MCU) including SRAM/ROM memory. The chip also supports rich peripheral interfaces, including SDIO, SPI master, I2C, I2S, IR input, UART, AUXADC, PWM, and GPIOs.

1.2 Features

1.2.1 Technology and Package

9mm x 8.7mm DRQFN package

1.2.2 Power Management and Clock Source

- Integrates high efficiency power management unit with single 3.3V power supply input
- Supports a 26-MHz crystal clock with low power operation in idle mode
- Supports an external 32-kHz crystal oscillator or internal 32-kHz for low power sleep mode

1.2.3 Platform

- ARM® Cortex-M33 MCU with FPU with up to 300MHz clock speed
- Supports up to 96KB for TCM and Cache memory
- Embedded 1MB SRAM
- Embedded 4MB pSRAM for applications
- Supports external serial flash with eXecute In Place (XIP) and on-the-fly AES
- Supports hardware crypto engines including AES, DES/3DES, SHA, ECC, TRNG for network security
- Supports up to 23 general purpose IOs, which are multiplexed with SPIm, UART, I2C, I2S, AUXADC, PWM and GPIO interfaces
- Supports 12 DMA channels

1.2.4 Wi-Fi

- IEEE 802.11 1T1R a/b/g/n/ac/ax 5 GHz and 2.4 GHz bands
- Supports 1x1 20MHz bandwidth, MCS0~8(256-QAM) in 2.4/5 GHz band
- Support MU-MIMO RX
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- Support Tx LDPC(Low-density parity check)
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- Wi-Fi security WFA WPA/WPA2/WPA3 personal
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- Integrated balun, PA, LNA, and T/R switch
- Support CSI (Channel Signal Information)
- Supports antenna diversity
- Optional external LNA and PA support

1.2.5 Bluetooth

- BT5.0 2M_PHY / Long Range / Advertising Extension / SAM / CS#2 / High Duty Cycle Non-Connectable ADV
- BT4.2 Link Layer Privacy / LE Secure Connection / LE Data Packet Length Extension / Link Layer Extended Scanner Filter Policies
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- BT4.0 BLE only mode
- Integrated balun and PA
- Up to 8 BLE links
- Packet loss concealment
- Channel quality driven data rate adaptation
- Channel assessment and WB RSSI for AFH
- Supports Bluetooth/Wi-Fi coexistence

1.2.6 Miscellaneous

- Embedded eFuse to store specific device information and RF calibration data
- Advanced TDD mode Wi-Fi/Bluetooth coexistence scheme

1.3 Block Diagram

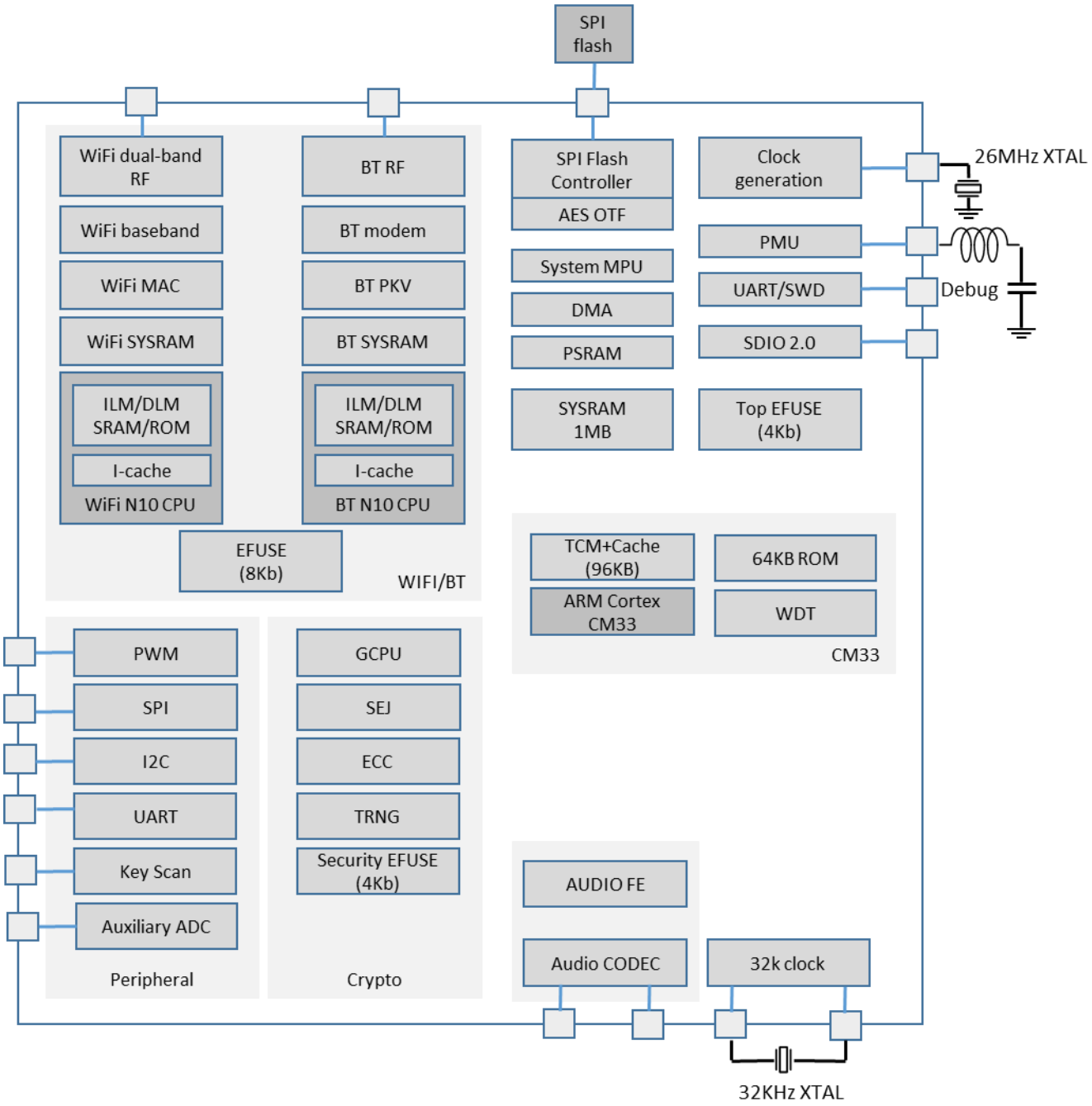


Figure 1-1 MT7931AN System-On-Chip block diagram

2 Functional Description

2.1 Power Management Unit

2.1.1 Introduction

PMU contains two buck converters: BUCK-D(for digital circuit), and BUCK-R (for RF circuit) and four LDOs: PHYLDO (for PLL), AUXLDO (for AUXADC), ALDO (for XTAL) and MLDO (for on-chip memory). Please refer to Figure 2-1. Power grid for more information.

2.1.2 Chip Power Plan

The 3.3V power source directly supplies the PMU, digital IOs (3.3V operation case), and the RF/AIP related circuitry. Figure 2-2 for PMU power on sequence.

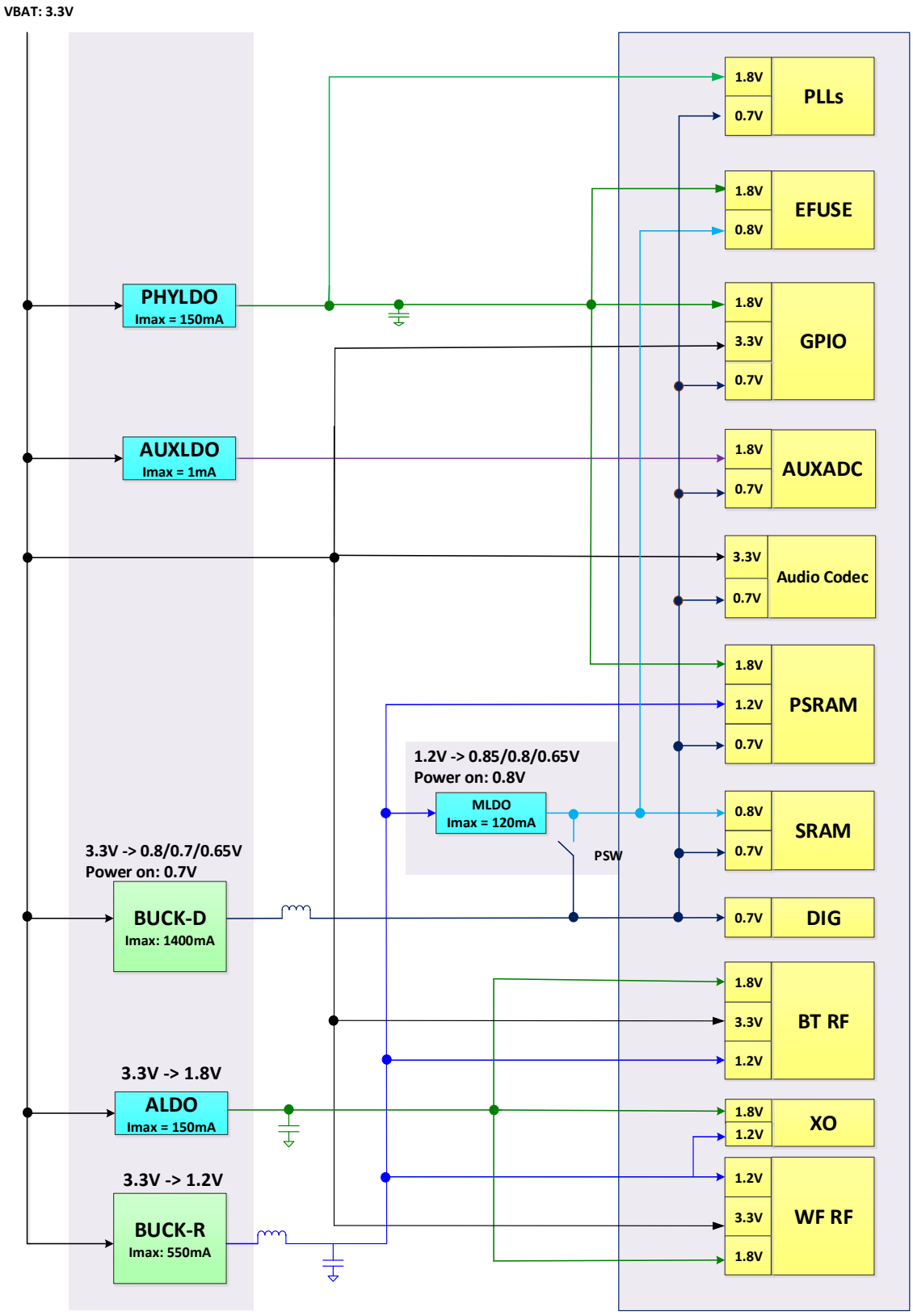
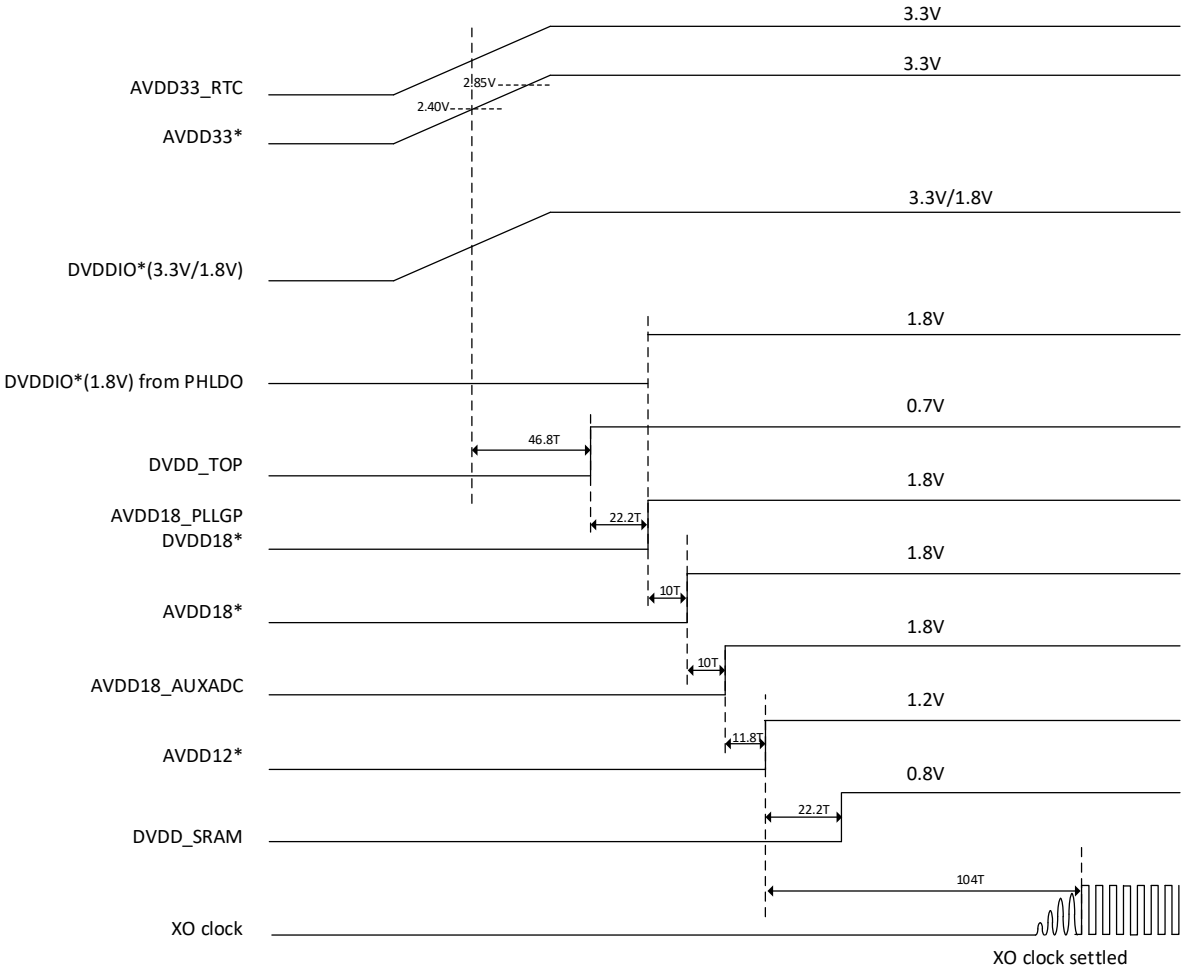


Figure 2-1 Power grid



*BGCLK 12.5kHz ±50% , 1T = max160us, min 53us

Figure 2-2 PMU power on sequence

2.1.3 Power Performance

Operation Mode		Test Conditions	Current Consumptions (1)	Unit
Power Mode	Scenario			
SLEEP	SLEEP_ext_32Khz	• Cortex-M33 in sleep state • TCM 96KB SRAM is retained • 1MB SYSRAM is retained • 32-kHz XTAL	370	µA
ACTIVE	Wi-Fi 2.4G TX	• N10 in active state • Cortex-M33 in active state • 96KB TCM is active • 1MB SYSRAM is active • 4MB PSRAM is active • 26-MHz XTAL	336@CCK 21.5 dBm 308@OFDM 20.5 dBm 222@HT20 17.5 dBm 202@HESU 16.5 dBm	mA
	Wi-Fi 5G TX		510@OFDM 21 dBm 372@HT20 17.5 dBm 354@HESU 16.5 dBm	mA
	Wi-Fi 2.4G RX		38@HT20 MCS0 39@HESU20 MCS8	mA
	Wi-Fi 5G RX		44@HT20 MCS0 47@HESU20 MCS8	mA
ACTIVE & SLEEP	DTIM = 1	• N10 in sleep state • Cortex-M33 in sleep state • 96KB TCM is retained • 1MB SYSRAM is retained • 4MB PSRAM is retained • 32-kHz XTAL	2.5 (beacon = 1.6ms)	mW

Note: The chip variation is +/- 25%.

(1) Conditions: VBAT and VDDIO at 3.3V, temperature at 25°C, typical corner IC, XTAL at 26 MHz

2.1.4 Power State

The MT7931AN platform has several power modes. You could switch the power mode depending on system use case. Please refer to Table 2-1.

Table 2-1 MT7931AN platform power modes

Power Modes	MCU clock	MCU bus	Wi-Fi/BT	Clock	SRAM / PSRAM	Peripheral	Wake Up Source	Wake Up Latency	Power Consumption
Active	300 MHz	Active	Off	PLL / XTAL	Active	On	---		12 mA[1]
Idle	Gated	Active	Off	PLL / XTAL	Active	On	All IRQ	< 1ms	8 mA[1]
Legacy Sleep (PSRAM On)	Gated	Gated	Off	XTAL	Sleep / On	On	All IRQ	< 1ms	2.5 mA
Deep Sleep	Power off	Power off	Off	External 32 kHz	Sleep	Power Off	Restricted IRQ[2]	< 10ms	0.37 mA

[1] The test condition is at 25°C and 3.3V. Power consumed by connectivity is not considered.

[2] List of modules available to signal IRQ as wake up source in deep sleep:

GPT(32K), SDIO slave, EINT, WIFI, BT, UART(CM33), RTC timer

2.2 System Initialization

MT7931AN system initialization is explained here in two subsections. The chip hardware power-on sequence is described in Section 2.2.1. The system boot up sequence after the secure boot master CM33 takes over the control is described in Section 2.2.3

2.2.1 Chip Power-On

This section explains the chip power-on sequence from 3.3V power supply getting stable to the fundamental chip hardware reset de-assertion (HW_CHIP_RST_B). After this fundamental chip hardware reset de-assertion, secure boot master CM33 takes over the system and boots from its ROM code.

After 3.3V power is stable, the BGCLK (band gap clock) in PMU starts to generate the 25-kHz fundamental clock, the first MT7931AN clock after power on. However, there is +/- 50% uncertainty out of this BGCLK such that this clock is only used for crystal clock control circuit. The power-on sequence is shown in the diagram below and is described in the following steps.

Step 1: 3.3V becomes stable and PMU BGCLK starts to work for PMU initialization

Step 2: After T-pmu (7.7 to 18ms), PMU will be valid and de-assert PMU_RST_N

Step 3: After PMU_RST_N de-assertion, XTAL control circuit will start to work

Step 4: After T-xtal (4.7 to 10.9ms), the crystal clock (XTAL_CLOCK) will be valid

Step 5: T-hwrst (4.7 to 14ms) guarantees that the XTAL_CLOCK is valid before HW_CHIP_RST_B

Step 6: After HW_CHIP_RST_B, IO setting CR will be auto-loaded from eFuse (8ms in 26 MHz)

Step 7: Secure boot master CM33 starts to boot from its ROM

Note that there is a dedicated hardware input pin SYS_RST_N which is also able to hold the chip reset state. However, this reset will always be de-asserted before PMU_RST_N if the application circuit on the PCB connects this pin to some RC circuit from 3.3V power supply.

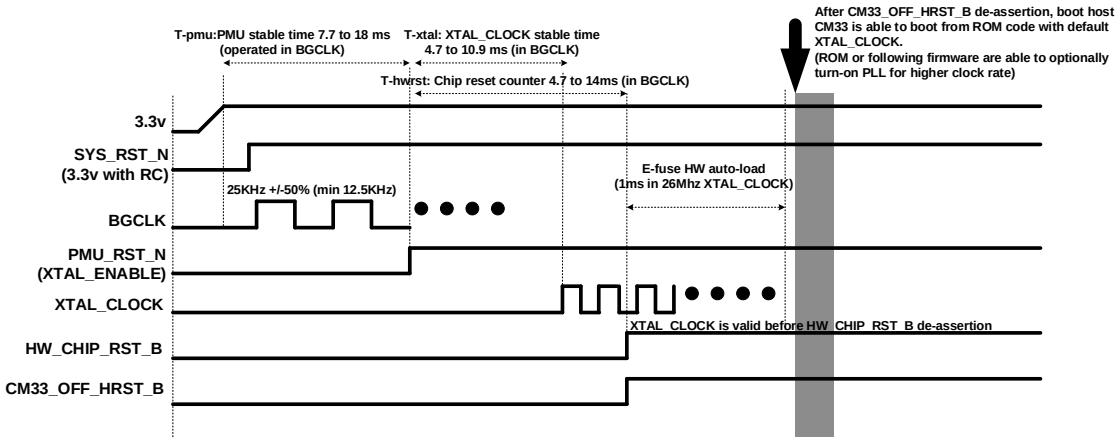


Figure 2-3 Power-On sequence

2.2.2 Bootstrap Function

The chip modes are sensed from the device pin during power up. After chip reset, the pull configurations are stored in a register and the settings determine the device operation mode.

Table 2-2 MT7931AN strapping pins and modes

Pin name	Pin description	Pin description	Description
GPIO_B_0	GPIO12	Chip Mode Sel	1: Normal mode: Connect 10kΩ to VCCIO_B 0: RSVD
GPIO_B_2	GPIO14	Download and Normal boot Sel	00: CM33 UART download mode 01: CM33 Flash normal boot mode 10: CM33 SDIO download mode 11: CM33 USB download mode e.g.01=GPIO_B_2 connects 10kΩ to GND, GPIO_B_12 connects 10kΩ to VCCIO_B
GPIO_B_12	GPIO24		
SF_QPI_CS	GPIO1	XTAL mode Sel	0: XTAL buffer mode 1: XTAL normal mode

Pins GPIO1, GPIO12, GPIO14, and GPIO24 are used for bootstrap. The system design should follow the following guidelines:

- Those pins shall not be used as input functions because the signals from other devices might affect the values sensed.
- Those pins shall not be used as an open-drain function because the pull-up resistor would affect the values

sensed.

- GPIO1 operating voltage is the same as the MT7931AN NOR flash operating voltage.
- GPIO12, GPIO14, and GPIO24 pins also act as GPIO pins; their operating voltages follow VCCIO_B .

2.2.3 System Boot Sequence

The system boot sequence after secure boot master CM33 reset de-assertion is described as below. CM33 will boot up first from BROM, and BROM code will verify security of bootloader and execute code directly on flash by XiP. Besides the boot loader, the flash code also contains the RTOS image for CM33, and the driver and firmware necessary for Wi-Fi and Bluetooth. By executing the boot loader, CM33 will verify the security of other flash codes, then jump to RTOS entry point on flash, and fetch the corresponding driver and firmware to enable Wi-Fi and Bluetooth.

The chip initial power state is by default set to ON for Cortex-M33 platform, crypto engine, infra bus and peripherals. But the chip initial state is by default set to OFF for Wi-Fi and Bluetooth. Thus, the boot sequence will take care of the power on procedure for those subsystems before enabling them.

2.3 Application Processor Subsystem Cortex-M33

The MCU subsystem consists of a 32-bit MCU, the AHB/APB bus matrix, internal RAM/ROM with ROM patch function, the flash controller and the system peripherals including Direct Memory Access (DMA) engine and the General Purpose Timer (GPT).

2.3.1 CPU

The MT7931AN features an ARM® Cortex-M33 processor, which is the most energy efficient ARM® processor currently available. It supports the clock rates up to 200MHz when core power is 0.7V and 300MHz when core power is 0.8V. The MCU executes the Thumb-2 instruction set for optimal performance and code size, including hardware division, single cycle multiplication and bit-field manipulation. The MT7931AN includes a Memory Protection Unit (MPU) in Cortex-M33 MCU to detect unexpected memory access and provide other memory protection features. The MT7931AN also includes FPU in Cortex-M33 MCU.

2.3.2 Cache and Tightly Coupled Memory

The MT7931AN has a cache for Cortex-M33 to improve the efficiency of the code and data fetched from the external flash. The only cacheable memory region is the external flash. The MT7931AN also has a Tightly-Coupled-Memory (TCM), a zero-wait-state memory dedicated to Cortex-M33 and can be accessed by Cortex-M33 exclusively. It is a memory space for the critical code, including interrupt service routines that need to be executed with minimum latency. The total size of cache memory and the TCM is 96KB. We offer four software-configurable options with different cache size, TCM size and cache associativity. You can choose the best option to maximize your application’s performance.

The cache system has the following features:

- Write-back (Unit: 4 words)
- Configurable 64/128/256-set, 4-way set associative (8KB/16KB/32KB)
- Each way has 64/128/256 cache lines with 8-word line size (2/4/8KB)
- 20-bit tag memory, including 19-bit high address and 1-bit valid bit
- 2-bit dirty memory. Each dirty bit records the dirtiness of half of the cache line, which is 4 words in this case.

The sizes of TCM and cache can be set to one of the following four configurations:

- 64KB TCM, 32KB cache (4-way, 256-set)
- 80KB TCM, 16KB cache (4-way, 128-set)
- 88KB TCM, 8KB cache (4-way, 64-set)
- 96KB TCM, 0KB cache (no cache)

2.4 Peripherals

2.4.1 Serial NOR Flash Controller

2.4.1.1 Introduction

The MT7931AN provides one serial NOR flash controller for the convenient access to the high-speed serial NOR flash device. The controller supports single-bit SPI serial NOR flash as well as high-performance dual-bit and quad-bit SPI serial NOR flash. The speed of SPI clock could be up to 60 MHz for quad-bit SPI.

2.4.1.2 Features

The serial NOR flash controller supports the following features:

- SPI bus compatible serial interface for common serial NOR flash device
- Map out 512-byte page program buffer, and support multi-page program
- Support SPI mode(single-bit) to transfer page program and 1-byte program
- Support 4-byte address mode, compatible 3-byte address mode
- Support single-bit read, dual output & dual I/O read and quad output & quad I/O read mode
- Read serial NOR flash data through direct read or PIO read mode
- Support serial NOR flash device frequency up to 60 MHz
- For direct read mode, the maximum supported capacity of serial NOR flash device is 2 Gbits. For PIO read modes, the maximum capacity is 4 Gbytes
- Support NOR flash device as follows: MX25U25635FMI, MX25U12835FMI, MX25U6432FM2I, W25Q64JW, W25Q128JW, W25Q256JW, MT25QU128
-

2.4.1.3 Block Diagram

The figure below shows the block diagram of serial NOR flash controller. It contains SNFC_Regs, SNFC_Prefetch, SNFC_Arb, SNFC_DMA and Direct_Read_Map. The SNFC_Regs is a register control module. The master system can access controller registers through APB interface. The SNFC_Prefetch allocates a buffer with 128x32-bit size for read and program process. In the read process, data is first transferred to the buffer and then sent to the read master. In the program process, the whole page data should be written to the buffer and the serial NOR flash controller delivers the data to serial NOR flash device; after that the page program is triggered. The SNFC_DMA is a HW engine to read data automatically from serial NOR flash and write data to SDRAM or SRAM through AXI bus. CPU must configure the source address, and start and end the destination address through SNFC_Regs module before DMA (SNFC_DMA) starts. The Direct_Read_Map module is used to translate the AXI master address to serial NOR flash memory address and responsible for returning data to CPU through AXI master. The SNFC_Arb takes the arbitration's mechanism when Direct Read_Map and SNFC_DMA access the serial NOR flash device simultaneously.

The serial NOR flash controller handles all commands, address, data sequence and serial interface protocols. It allows users to read serial NOR flash in three ways: PIO read mode, DMA read mode and direct read mode.

1. For PIO read mode, CPU could program control registers (SNFC_Regs) in a specific sequence and get the serial NOR-flash data through APB. This PIO read mode is usually used for reading data of few bytes

2. For DMA read mode, the SNFC_DMA copies serial NOR flash data to SDRAM or SRAM through AXI bus

3. For direct read mode, the CPU could directly read serial NOR flash data through AXI bus by address offset

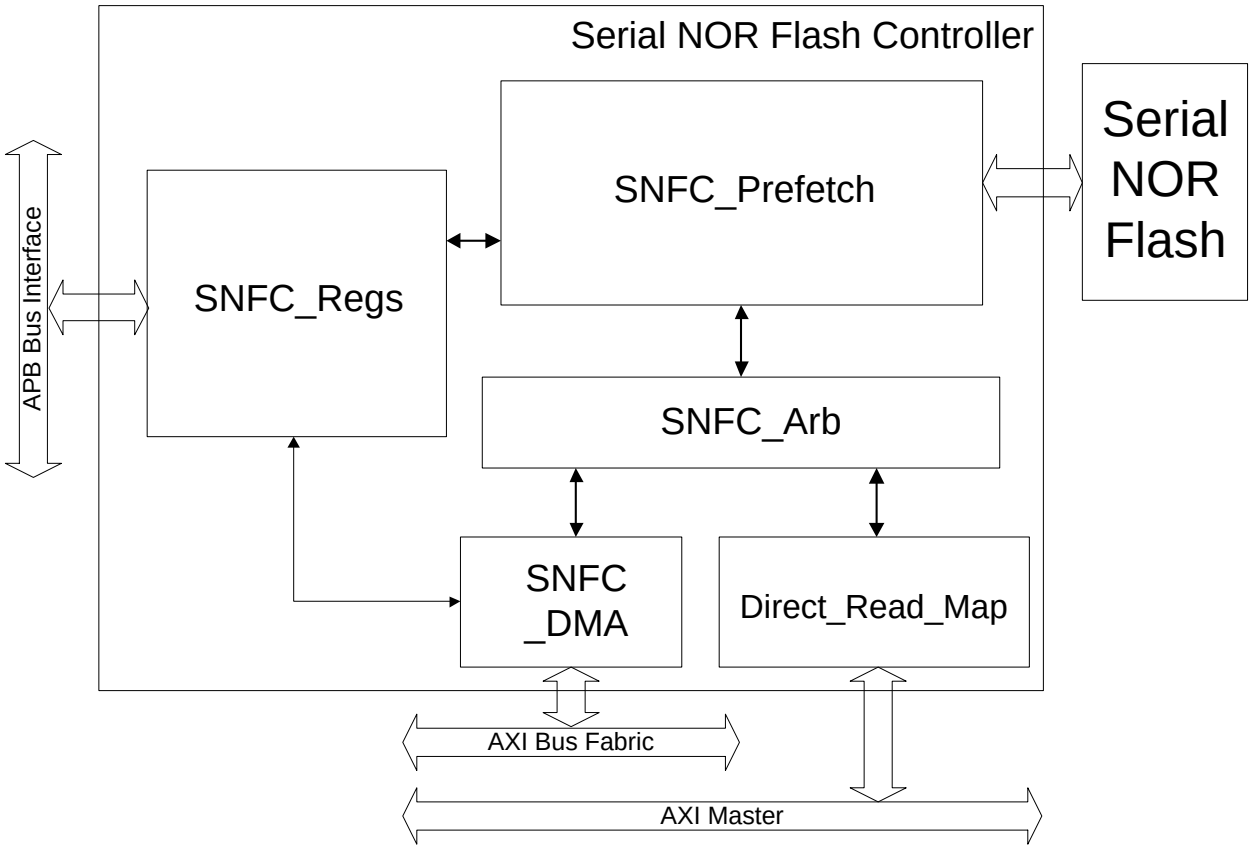


Figure 2-4. Serial NOR flash controller block diagram

2.4.1.4 Read Flash

The standard SPI link format is combined with command, address and data bytes. The read operation format of single-bit SPI mode is shown in the following figure.

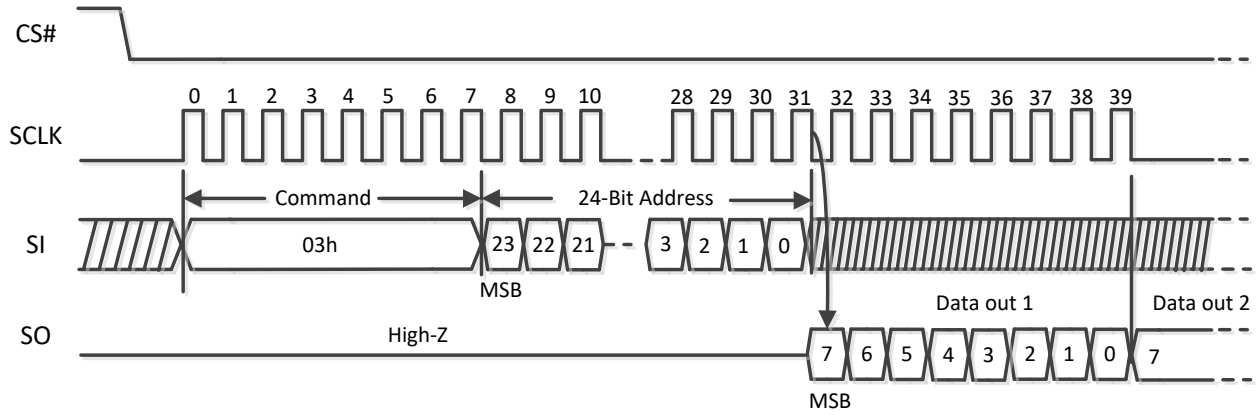


Figure 2-5. Read operation sequence

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2.4.2 Auxiliary ADC Function

2.4.2.1 Functional description

The MT7931AN features one auxiliary ADC function. The ADC function contains an 8-channel analog switch, a single-end input asynchronous 12-bit SAR (Successive Approximation Register) ADC, dithering function and a digital averaging function.

The digital averaging function can perform on-the-fly averaging function of 1/2/4/8/16/32/64 points.

The ADC features the dithering function to enhance the DNL performance.

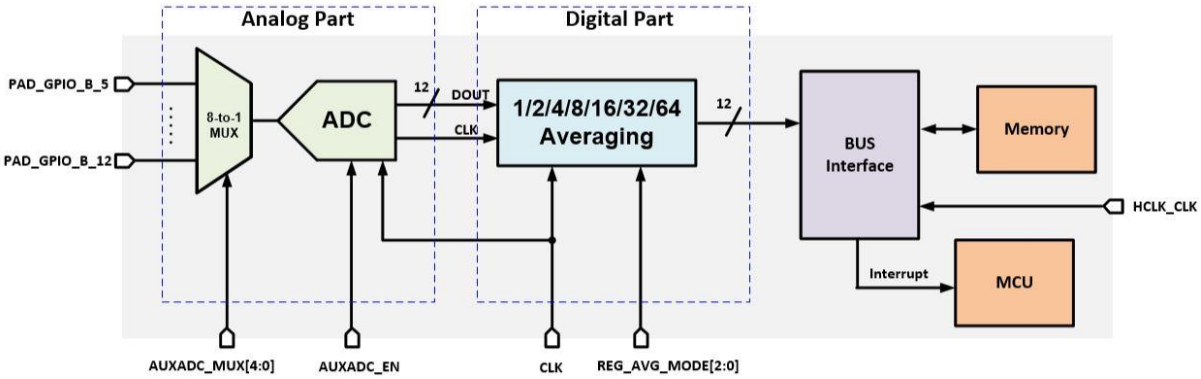

Figure 2-6 Auxiliary ADC block diagram

2.4.2.2 Features and IO

The features of auxiliary ADC are listed below:

- Input channel number: 8 channels
- Sampling and output data rate: 2MS/s (default)
- DNL without dithering and averaging: <±2LSB
- DNL with dithering and averaging: <±1LSB
- Dithering function: 16 levels with step size of 4LSB

The IOs of auxiliary ADC can be set as either analog IO for ADC function or digital IO for GPIO function:

- Analog Mode: Used for ADC application. Input voltage is 1V.
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-
-
-
-

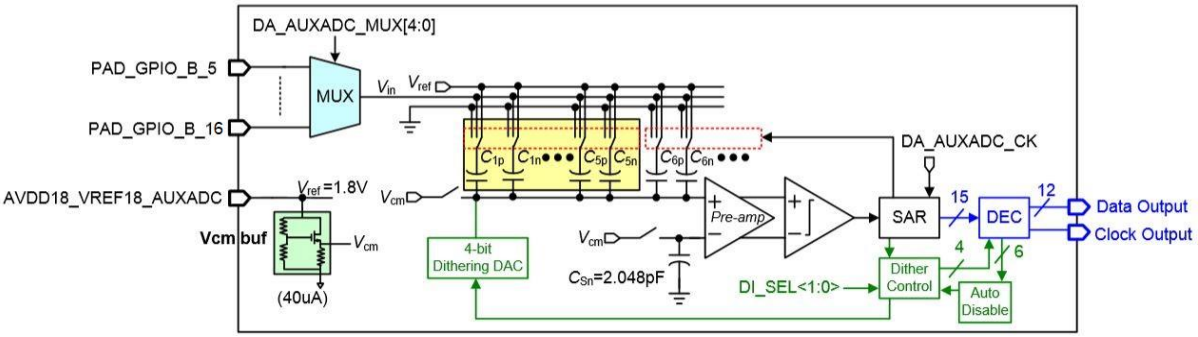


Figure 2-7 Auxiliary ADC analog IP block diagram

2.4.3 SPI Master Controller

2.4.3.1 Functional Description

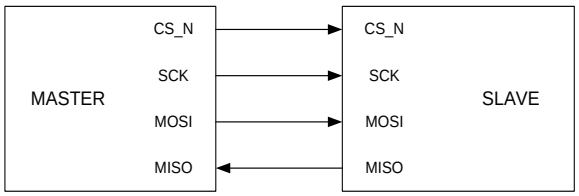


Figure 2-8 Pin connection between SPI master and SPI slave

The SPI interface is a bit-serial, four-pin transmission protocol. The above figure is an example of the connection between the SPI master and SPI slave. The SPI interface controller is a master responsible for the data transmission with the slave.

2.4.3.2 Pin Description

Table 2-3 SPI controller interface

Signal name	Type	Description
CS_N	O	Low active chip selection signal
SCK	O	The (bit) serial clock
MOSI	O	Data signal from master output to slave input
MISO	I	Data signal from slave output to master input

2.4.3.3 Transmission Formats

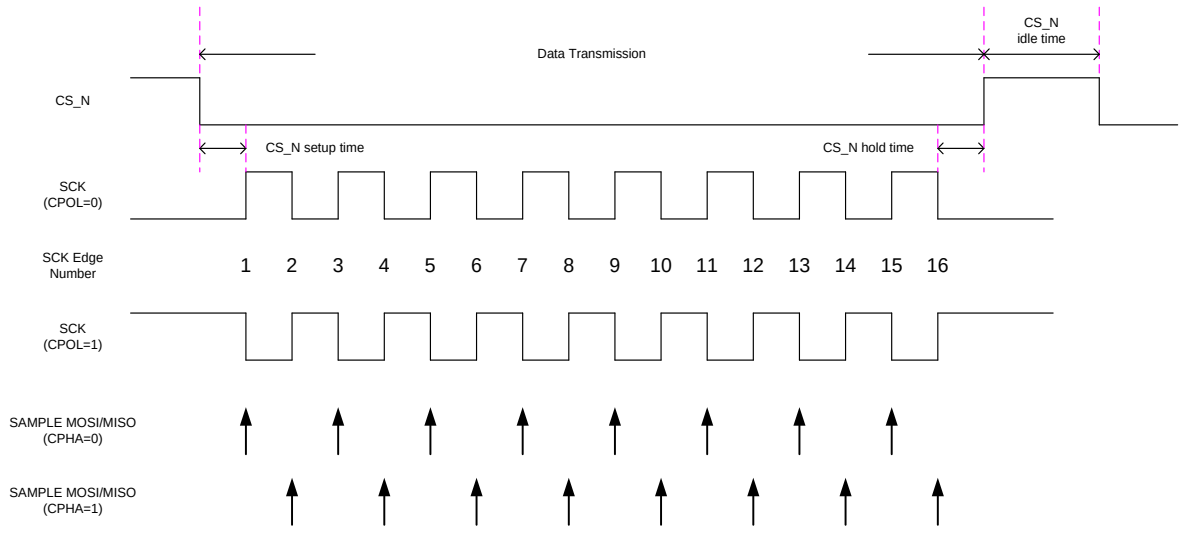


Figure 2-9 SPI transmission formats

The above figure shows the waveform during the SPI transmission. The low active CS_N determines the start point and end point of one transaction. The CS_N setup time, hold time and idle time are also depicted.

CPOL defines the clock polarity in the transmission. Two types of polarity can be adopted, i.e. polarity 0 and polarity 1. The above figure is an example of both clock polarities (CPOL).

CPHA defines the legal timing to sample MOSI and MISO. Two different methods can be adopted.

2.4.3.4 Features

The features of the SPI controller (master) are:

- Configurable CS_N setup time, hold time and idle time
- Programmable SCK high time and low time
- Configurable transmitting and receiving bit order
- Two configurable modes for the source of the data to be transmitted. 1) In Tx DMA mode, the SPI controller automatically fetches the transmitted data (to be put on the MOSI line) from memory. 2) In Tx FIFO mode, the data to be transmitted on the MOSI line are written to FIFO before the start of the transaction.
- Two configurable modes for destination of the data to be received. 1) In Rx DMA mode, the SPI controller automatically stores the received data (from MISO line) to memory. 2) In Rx FIFO mode, the received data keep being in Rx FIFO of the SPI controller. The processor must read back the data by itself.
- Adjustable endian order from/to memory system
- Programmable byte length for transmission
- Unlimited length for transmission. This is achieved by the operation of PAUSE mode. In PAUSE mode, the CS_N signal will keep being active (low) after the transmission. At this time, the SPI controller is in PAUSE_IDLE state, ready to receive the resume command. The state transition is shown in **錯誤! 找不到參照來源。**10
- Configurable option to control CS_N deassert between byte transfers. The controller supports a special transmission format called CS_N deassert mode. Figure 2-122 illustrates the waveform in this transmission format.

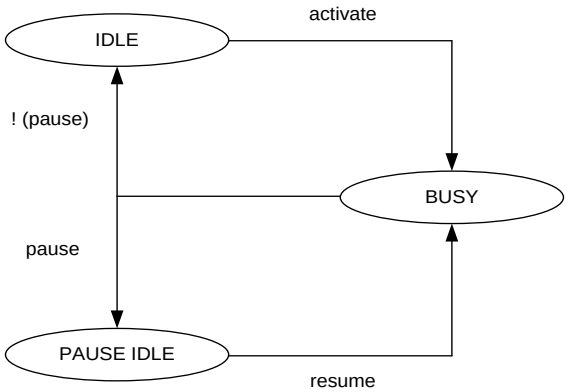


Figure 2-10 Operation flow with or without PAUSE mode

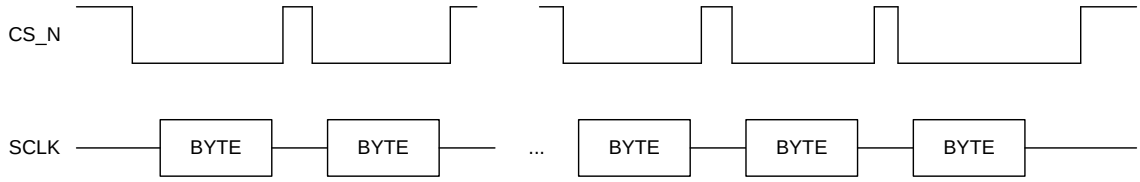


Figure 2-11 CS_N deassert mode

2.4.4 SDIO Slave

2.4.4.1 Functional Description

The SD Input/Output (SDIO) card is based on and compatible with the SD memory card. The controller fully supports the SD memory card bus protocol as defined in SD Memory Card Specification Part 1 Physical Layer Specification version 2.0 and SDIO Specification version 2.0.
SDIO provides high-speed data IO with low power consumption. SDIO module provides an SDIO2.0 card interface connected to the host and can support multiple speed modes including default speed mode and high speed mode.

2.4.4.2 Features

- SDIO 2.0 basic features
  - 1-bit and 4-bit SD data transfer modes
  - Default mode: Variable clock rate 0-25MHz, up to 12.5MB/sec interface speed (using 4 parallel data lines)
  - High-Speed mode: Variable clock rate 0-50 MHz, up to 25MB/sec interface speed (using 4 data lines)
- CR and data port access
  - Supports control register (CR) port single read/write access (AHB slave)
  - Supports data port single and burst read/write access (AHB master)
- DMA function
  - One TX channel and two Rx channels
  - Moves TX data from HIF buffer to SYSRAM, TCM
  - Moves RX data or firmware prepared data from SYSRAM, TCM to HIF buffer

2.4.4.3 Block Diagram

The block diagram of the SDIO controller is shown in Figure 2-12

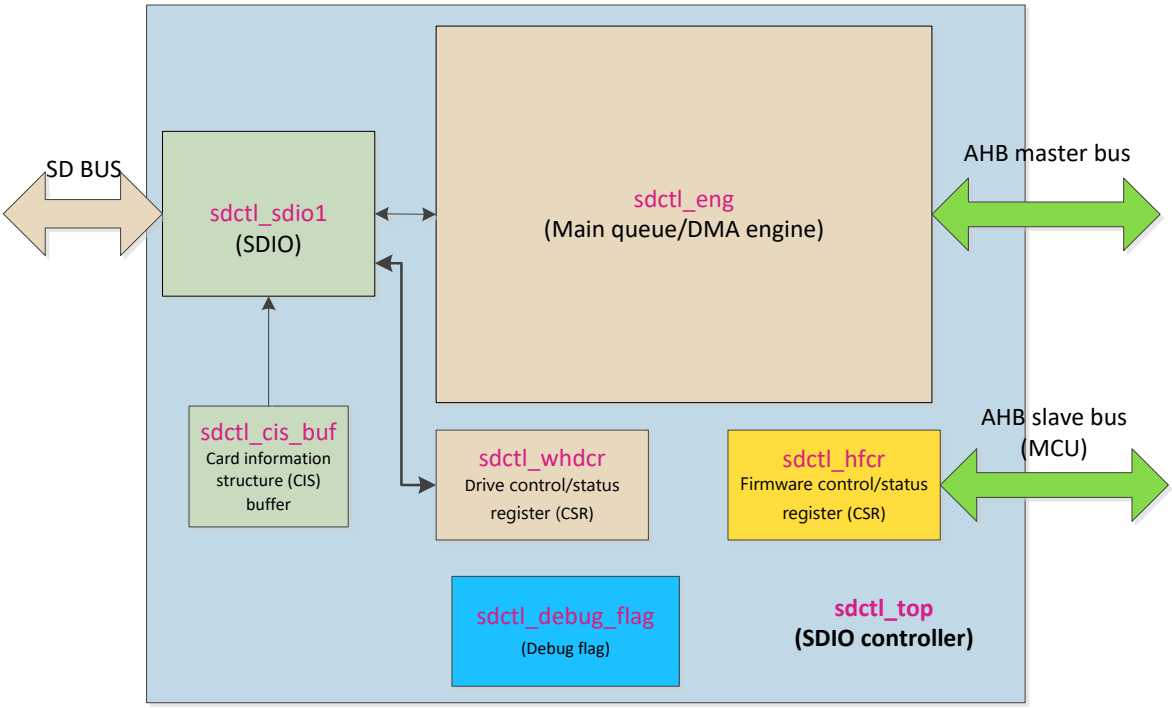


Figure 2-12 SDIO controller block diagram

2.4.4.4 Functions Description

From the external view, the SDIO interface mainly includes the SD bus and AHB master and slave. The AHB master is used for DMA operations and the AHB slave is used for register access from the MCU. The SD bus provides an interface for SD specification.

2.4.4.5 Pin description

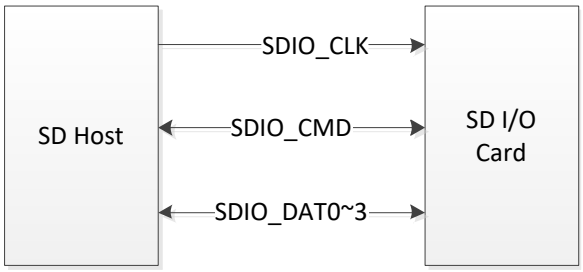


Figure 2-13 Signal connections to 4-bit SDIO cards

Table 2-4 SDIO pin definitions

Pin	Name	SD 4-bit mode		SD 1-bit mode	
1	SDIO_DAT3	DAT[3]	Data line3	N/C	Not used
2	SDIO_CMD	CMD	Command line	CMD	Command line
3	VSS1	VSS1	Ground	VSS1	Ground
4	VDD	VDD	Supply voltage	VDD	Supply voltage
5	SDIO_CLK	CLK	Clock	CLK	Clock
6	VSS2	VSS2	Ground	VSS2	Ground
7	SDIO_DAT0	DAT[0]	Data line0	DATA	Data line
8	SDIO_DAT1	DAT[1]	Data line1 or interrupt	IRQ	Interrupt
9	SDIO_DAT2	DAT[2]	Data line2	RW	Not used

2.4.4.6 SDIO Timing Waveform (3.3V)

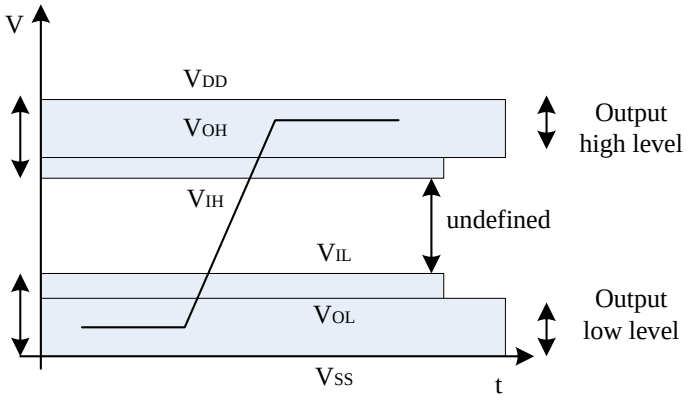


Figure 2-14 Bus signal levels

Table 2-5 Bus signal voltage

Parameter	Symbol	Min.	Max.	Unit	Conditions
Output High Voltage	VOH	0.75*VDD		V	IOH=-2mA VDD min
Output Low Voltage	VOL		0.125*VDD	V	IOL = 2mA VDD min
Input High Voltage	VIH	0.625*VDD	VDD+0.3	V	
Input Low Voltage	VIL	Vss-0.3	0.25*VDD	V	

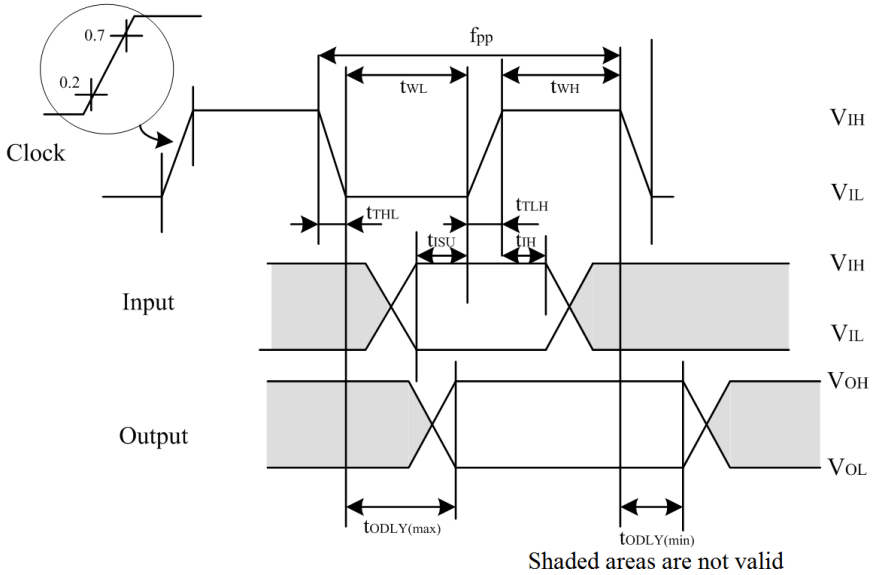


Figure 2-15 Bus timing diagram (default)

Table 2-6 Bus timing parameter values (default)

Parameter	Symbol	Minimum	Maximum	Unit	Remark
Clock CLK (All values are referred to min (VIH) and max (VIL)					
Clock frequency data transfer mode	fPP	0	25	MHz	CCARD ≤ 10 pF (1 card)
Clock frequency identification mode	fOD	0/100	400	kHz	CCARD ≤ 10 pF (1 card)
Clock low time	tWL	10		ns	CCARD ≤ 10 pF (1 card)
Clock high time	tWH	10		ns	CCARD ≤ 10 pF (1 card)
Clock rise time	tTLH		10	ns	CCARD ≤ 10 pF (1 card)
Clock fall time	tTHL		10	ns	CCARD ≤ 10 pF (1 card)
Inputs CMD, DAT (referred to CLK)					
Input set-up time	tISU	5		ns	CCARD ≤ 10 pF (1 card)
Input hold time	tIH	5		ns	CCARD ≤ 10 pF (1 card)
Outputs CMD, DAT (referred to CLK)					
Output delay time during data transfer mode	tOLDY	0	14	ns	CL ≤ 40 pF (1 card)
Output delay time during identification mode	tOLDY	0	50	ns	CL ≤ 40 pF (1 card)

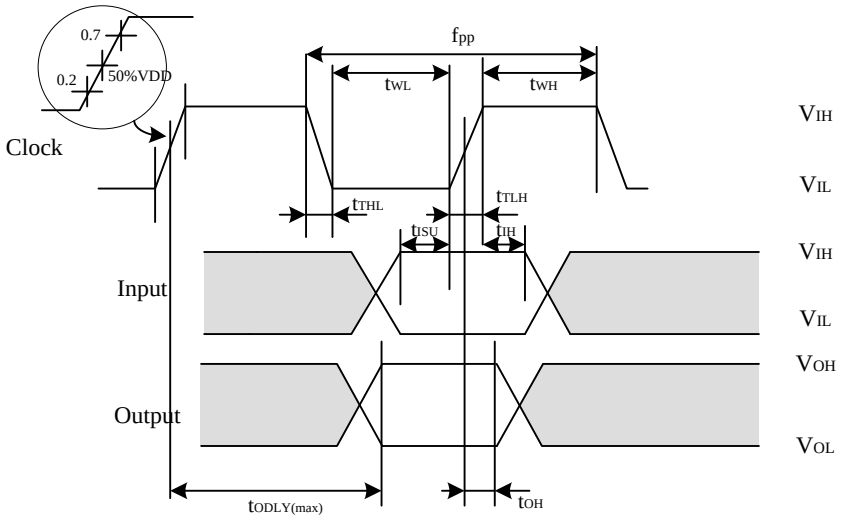


Figure 2-16 High-speed timing diagram

Table 2-7 High-speed timing parameter values

Parameter	Symbol	Minimum	Maximum	Unit	Remark
Clock CLK (All values are referred to min (VIH) and max (VIL)					
Clock frequency data transfer mode	fPP	0	50	MHz	CCARD ≤ 10 pF (1 card)
Clock low time	tWL	7		ns	CCARD ≤ 10 pF (1 card)
Clock high time	tWH	7		ns	CCARD ≤ 10 pF (1 card)
Clock rise time	tTLH		3	ns	CCARD ≤ 10 pF (1 card)
Clock fall time	tTHL		3	ns	CCARD ≤ 10 pF (1 card)
Inputs CMD, DAT (referred to CLK)					
Input set-up time	tISU	6		ns	CCARD ≤ 10 pF (1 card)
Input hold time	tIH	2		ns	CCARD ≤ 10 pF (1 card)
Outputs CMD, DAT (referred to CLK)					
Output delay time during data transfer mode	tOLDY		14	ns	CL ≤ 40 pF (1 card)
Output hold time	tOH	2.5		ns	CL ≥ 40 pF (1 card)
Total system capacitance for each line (1)	CL		40	pF	1 card

(1) In order to satisfy the serving time, the host shall drive only one card.

2.4.5 I2C

2.4.5.1 Introduction

There are two I2C master channels in the MT7931AN with the same HW architecture. I2C is a two-wire serial interface with two signals, SCL and SDA. SCL is a clock signal driven by the master. SDA is a bi-directional data signal that can be driven either by the master or by the slave. This generic controller supports the master role and conforms to the I2C specification.

2.4.5.2 Features

The main supported features of I2C Master are as follows:

- I2C compliant master mode operation
- Adjustable clock speed for Fast-mode Plus
- 7-bit address
- Clock stretching feature
- START/STOP/repeated START conditions
- I2C_FIFO mode
- DMA transfer mode
- Multi-write per transfer
- Multi-read per transfer

- Multi-transfer per transaction
- Combined format transfer with length change capability
- Multi-transfer with repeated START condition

2.4.5.3 Block Diagram

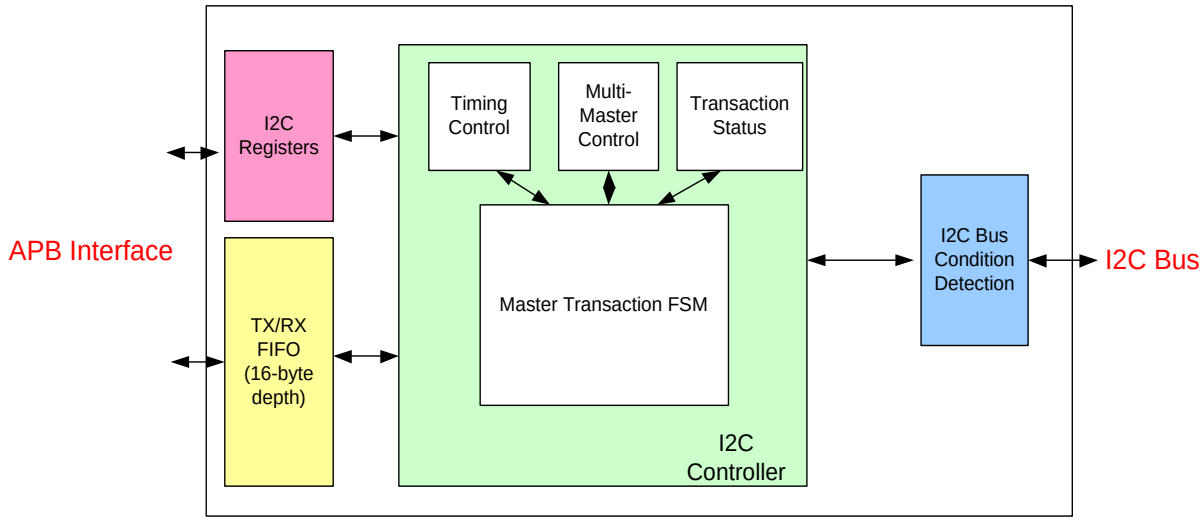


Figure 2-17 Block diagram of I2C

- I2C Registers: I2C configuration and status registers.
- Tx/Rx FIFO: Store the data to be sent to I2C slave or the data received from I2C slave.
- Master Transaction FSM: I2C master finite-state machine used to indicate the current transfer stage.
- Timing Control: Control the frequencies of SCL according to the configuration of CLOCK_DIV , SAMPLE_CNT_DIV and STEP_CNT_DIV.
- Multi-Master Control: Execute arbitration when multiple masters exist on the I2C bus.
- Transaction Status: Record the number of bytes that has been transferred and the number of transfers that has been done. It can be used to judge if all transactions have been completed.
- I2C Bus Condition Detection: Detect START/STOP/repeated START conditions and clock stretching on the I2C bus.

2.4.6 UART

2.4.6.1 Introduction

The UART controller provides full duplex serial communication channels between the MT7931AN chip and external devices. The UART controller has M16C450 and M16550A operation modes, which are compatible with a range of standard software drivers. The extensions are designed to be broadly software compatible with 16550A variants, but certain areas offer no consensus.

In common with the M16550A, the UART controller supports word lengths from 5 to 8 bits, an optional parity bit and one or two stop bits, and this word length is fully programmable by a CPU interface. A 16-bit programmable baud rate generator and an 8-bit scratch register are included, along with separate transmission and received FIFOs. Eight modem control lines and a diagnostic loop-back mode are provided. The UART_TOP also includes two DMA handshake lines which are used to indicate when the FIFOs are ready to transfer data to the CPU. Interrupts can be generated from any of the several sources.

After hardware reset, the UART controller is in M16C450 mode. Its FIFOs can be enabled and the UART controller can enter M16550A mode. The UART controller adds further functionality beyond M16550A mode. Each of the extended functions can be selected individually under software control.

2.4.6.2 Features

- Provide 4 channels of UART controller
- UART_TOP0, UART_TOP1 and CM33_UART are 4-pin (TX, RX, CTS, RTS) UART_TOP channel
- Support both M16C450 and M16550A operation modes
- Compatible with standard software drivers
- Transfer system: Asynchronous
- Data length: 5 to 8 bits
- Hardware flow control: CTS/RTS-based automatic transmission and reception of control
- Software flow control: Use special character XON/XOFF to do software flow control
- Baud rate is programmable from 300 bps to 3 Mbps
- Baud rate error: Less than 0.25 %
- Interrupt request: Receive interrupts/transmit interrupts
- Data transfer: DMA (Transmit/Receive) transfer is supported

2.4.7 PWM

2.4.7.1 Functions Description

The MT7931AN features 2 generic PWMs to generate pulse sequences with programmable frequency and duration for LCD, vibrators, and other devices.

The PMU features three configurable pattern options.

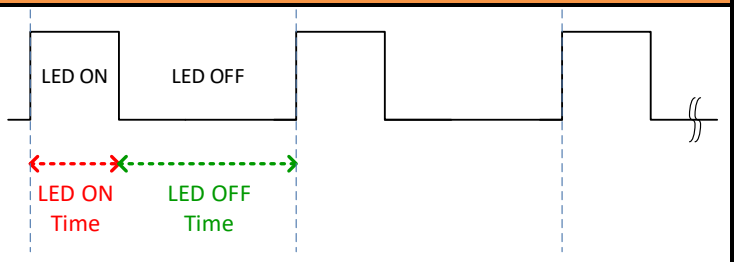
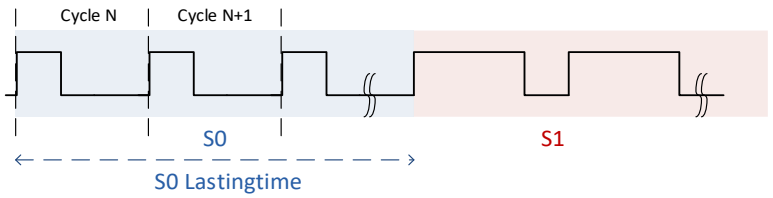
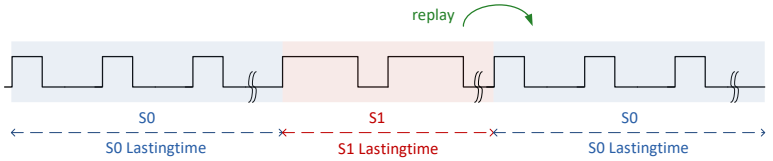
Mode	Description	Waveform
1	Basic PWM: LED ON time (duration) and LED OFF time (duration) are configurable.	
2	Two-State PWM: There are two configurable states (S0 and S1) for PWM LED.	
3	Two-State replay mode: Users can set replay mode with specified S1_Lasting_Time. PWM LED would act as [S0 -> S1 -> S0 -> S1 -> S0 ….] with period time of (S0_Lasting_Time + S1_Lasting_Time)	

Figure 2-18 PWM patterns

2.4.8 DMA

Direct memory access (DMA) is used to transfer data between memory and memory as well as memory and peripherals without MCU interventions.

2.4.8.1 Command Queue (CQ) DMA

The purpose of CQ_DMA is to perform data transfer between memory and memory without CPU interventions.

The supported features of CQDMA are as below:

- Up to three channels of simultaneous data transfer are supported.
- Comply with the system bus (AXI).
- Two out-standings for three channels
- Source or destination address fix mode
- Source or destination address-wrapping mode
- Source and destination address-increment mode
- Fix-pattern mode
- Bandwidth limiter
- TrustZone
- Round-Robin (RR) for scheduling scheme

2.4.8.2 Application Processor (AP) DMA

The purpose of APDMA is to perform data transfer between memory and peripherals.

The supported features of APDMA are as below:

- Up to 9 channels of simultaneous data transfer are supported.
- Comply with the system Bus (AXI)
- TrustZone
- Interrupt notification
- Round-Robin (RR) for scheduling scheme

There are 2 types of DMA channels supported in MT7931AN.

- Peripheral DMA: The behavior of Peripheral DMA is like that of CQ-DMA. The major difference is that the source or destination is peripherals FIFO, not memory.
- Virtual FIFO DMA (VFF DMA): It’s a peripheral DMA with an additional FIFO control engine. It is used to provide the buffering capacity for peripherals.

2.4.8.2.1 Peripheral DMA

The behavior of Peripheral DMA is like that of CQ-DMA. The major difference is that the source or destination is peripheral FIFO, not memory. And there are handshaking signals (REQ / ACK) between DMA and peripheral. Because of handshaking signals, the DMA channels with corresponding peripheral channels are fixed.

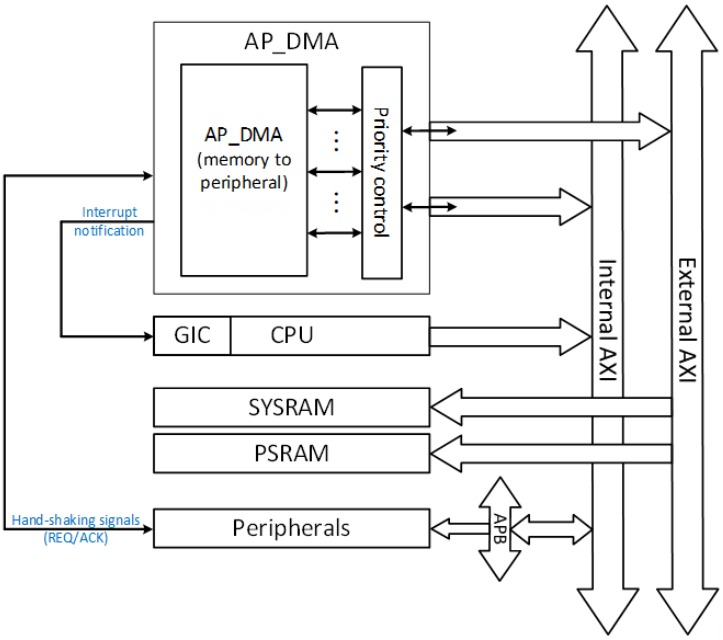


Figure 2-19 APDMA Block Diagram

2.4.8.2.2 Virtual FIFO

Virtual FIFO DMA is designed to offload the control of the serial interface. The difference between the virtual FIFO DMA and the peripheral DMA is that the virtual FIFO DMA contains an additional FIFO controller.
VFF is like the ring buffer, and uses two address pointers (VFF_WPT/VFF_RPT) to control VFF condition. According to these two address pointers, two symbols are defined (VFF_VALID_SIZE/VFF_LEFT_SIZE) to represent the valid data and available space in VFF.
The figure below illustrates the operations of virtual FIFO DMA used for UART RX.

(1) READ: DMA controller reads data from UART and increments the WRITE pointer of the FIFO controller.
(2) WRITE; DMA controller writes data that was area from UART to SRAM in the area defined before enabling the virtual FIFO.
(3) READ: MCU reads data when FIFO is not empty and the amount of data is over a pre-defined threshold. The read transaction will be finished only when DMA controller reads back the data from SRAM.
(4) READ: DMA controller reads data from SRAM and increments the READ pointer of the FIFO controller.

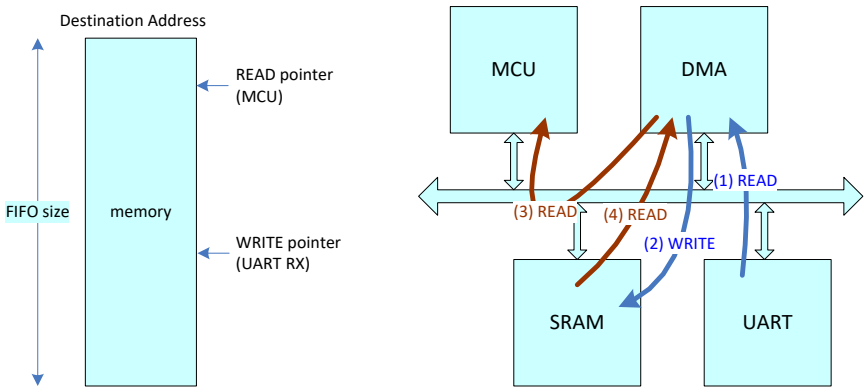


Figure 2-20 Virtual FIFO Concept

2.4.8.2.3 APDMA Channels and Priority Control

There are totally 7 virtual FIFO DMA channels and 2 peripherals DMA channels in MT7931AN.

Table 2-8 DMA type for hardware IP

Hardware IP	DMA Type
Radio (Bluetooth)	Virtual FIFO DMA x 2
UART (x2)	Virtual FIFO DMA x 4
AUXADC	Virtual FIFO DMA x 1
I2C	Peripheral DMA x 2

2.4.9 GPT

2.4.9.1 Introduction

The Application Processor X General Purpose Timer (APXGPT) module includes five 32-bit GPTs and one 64-bit GPT. Each GPT supports four operation modes, which are ONE-SHOT, REPEAT, KEEP-GO and FREERUN. Each GPT can be operated on one of the two clock sources, RTC clock (32.768 kHz) or system clock (13 MHz).

2.4.9.2 Features

Table 2-9 provides the detailed information about the four operation modes for the GPT, ONE-SHOT, REPEAT, KEEP-GO and FREERUN.

Table 2-9 Operation Mode of GPT

Mode	Auto Stop	Interrupt Supported	Counting Behavior	When GPTn_COUNT equals GPTn_COMPARE	Example: Compare value is set to 2 (The bold value means interrupt asserted)
ONE-SHOT	Yes	Yes	The GPT stops counting when GPTn_COUNT equals GPTn_COMPARE	EN is reset to 0	0,1,**2**,2,2,2,2,2,2,2,2,2,…
REPEAT	No	Yes	The GPT count is reset to 0 when GPTn_COUNT equals GPTn_COMPARE	Count is reset to 0	0,1,**2**,0,1,**2**,0,1,**2**,0,1,**2**…
KEEP-GO	No	Yes	The GPT count is reset to 0 when overflow occurs		0,1,**2**,3,4,5,6,7,8,9,10,…
FREERUN	No	No	The GPT count is reset to 0 when overflow occurs		0,1,2,3,4,5,6,7,8,9,10,…

Note:
Each timer’s operation is independent and can be programmed to select the clock source, RTC clock (32.768 kHz) or system clock (13 MHz). After the clock source is determined, the division ratio of the selected clock can be programmed. The division ratio can be fine-granulated as 1 to 13 and coarse-granulated as 16, 32 and 64.

2.4.9.3 Block Diagram

APXGPT consists of five sets of 32-bit GPTs and one set of 64-bit GPTs.
When the GPT triggers an IRQ, it will also issue a wakeup signal to "Sleep Control", and then “Sleep Control” can wake the MCU if the MCU is in sleep mode.

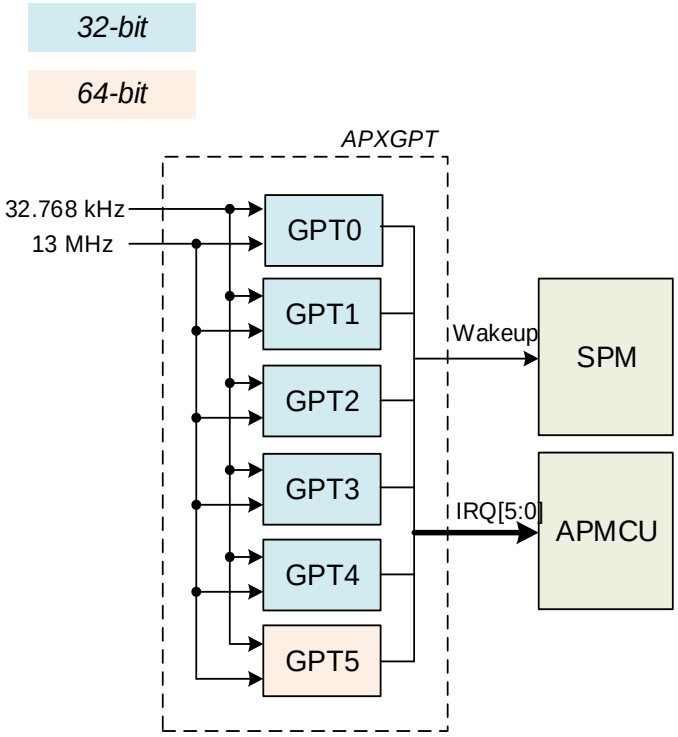


Figure 2-21 Block Diagram of APXGPT

2.4.9.4 Theory of Operations

For the GPT5 64-bit timer, the read operation of the 64-bit timer value will be separated into 2 APB reads since an APB read is of 32-bit width. To perform the read operation of 64-bit timer value, the lower word should be read first and then the higher word. The read operation of the lower word will freeze the “read value” of the higher word but will not freeze the timer counting. This ensures that the separated read operation acquires the correct timer value.

To program and use the GPT, please note:
The counter value can be read at any time when the clock source is system clock.
The counter value can be read at any time even when the clock source is RTC clock.
The comparative value can be programmed at any time. When the comparative value is rewritten during count operation, the counter will be reset to 0 and restart counting.

2.4.10 WDT

2.4.10.1 Introduction

The MT7931AN features a watchdog timer (WDT) for the Arm Cortex-M33 processor (referred to as CM33 in this document). CM33_WDT is the watchdog timer for the Cortex-M33 processor. When the Cortex-M33 processor hangs due to some malfunctions, the watchdog timer is used to generate system alarm and trigger whole chip reset.

2.4.10.2 Functional Description

The WDT provides the counter with the clock source of 32 kHz and asserts interrupt when needed. There is an interrupt counter, and it can operate as follows:

- One-shot mode: the timer stops when the timer counts down to zero.
- The timer counts from a programmable initial value and asserts interrupt when counting to zero. The interrupt will be level active low. The unit of the counter can be 1 x 32 kHz cycle.
  The WDT provides two ways to generate the WDT event.
- Triggered by the time-out event to configure WDT HW reset mode.
- The WDT has an 11-bit counter and uses the 32-kHz clock. The software regularly restarts the timer to prevent it from expiring. If the timer fails to restart the WDT, it will expire and generate a WDT event.
- The programmable period length is 32ms*(1~2048) which is ranged from 32ms to 65.5s.
- Triggered by software programming to write SW reset KEY.

2.4.10.3 Event Notification for CM33

The WDT provides the following options when a WDT event is generated.

- Trigger whole chip reset
- Interrupt itself

Note: The reset whole chip option is included in top chip reset register space.

The WDT module can only be reset by the external reset (SYS_RST_N) and the PMU reset. Some WDT control registers feature a key protection mechanism to prevent unintentional access.

2.4.11 GPIO

2.4.11.1 Overview

The MT7931AN platform offers 23 General-Purpose Input/Output (GPIO) pins. By setting the control registers, the MCU software can control the direction and the output value of the GPIO pins and read the input value of these pins. The GPIO pins and GPO (General-Purpose Output) pins are multiplexed with other functions to reduce the pin count.

The clock to send data outside the chip is software configurable. There are six clock-out ports and each clock-out port can be programmed to output the appropriate clock source. In addition, when two GPIO pins function for the same peripheral IP, the smaller GPIO serial number has higher priority over the bigger one.

Figure 2-22 shows the block diagram of the GPIO controller in the MT7931AN.

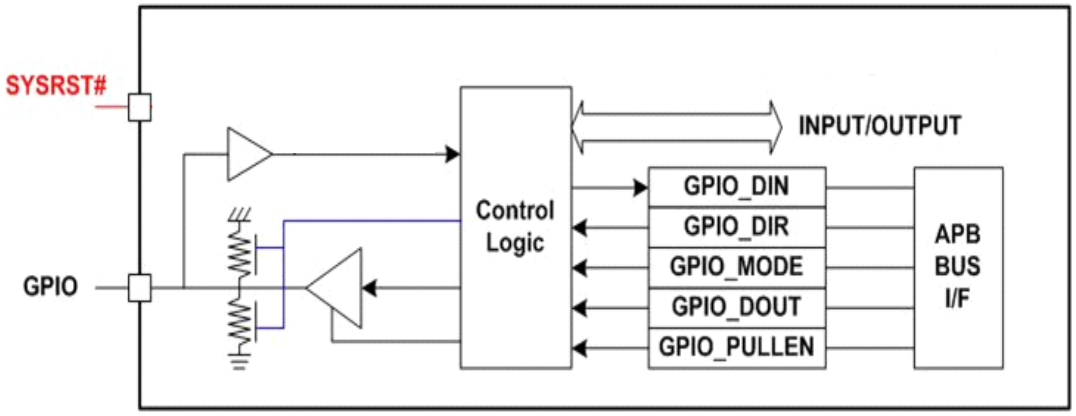


Figure 2-22 MT7931AN GPIO Controller

2.4.11.2 I/O Pull up or Down Control Truth Table

All MT7931AN GPIO pins support both 1.8V and 3.3V IO power and different Pull up/Pull down resistors can be selected as Table 2-10.

Table 2-10 PU/PD resistance Spec

E	PUPD	R1	R0	R Value of 1.8V/3.3V IO Power
0	0	0	0	High-Z
0	0	0	1	PU10Kohm
0	0	1	0	PU50Kohm
0	0	1	1	PU10Kohm//50Kohm
0	1	0	0	High-Z
0	1	0	1	PD10Kohm
0	1	1	0	PD50Kohm
0	1	1	1	PD10Kohm//50Kohm
1	X	X	X	High-Z

2.5 Interrupt

2.5.1 Introduction

The MT7931AN embeds an interrupt controller, which is composed of an NVIC (Nested Vectored Interrupt Controller), a WIC (Wakeup Interrupt Controller) and a de-bounce circuit. The WIC and de-bounce circuit are in the Always-On domain. All internal or external interrupts are connected to the WIC as well as to the NVIC; thus, each interrupt signal can serve as wakeup source for the CM33 processor. And these interrupt sources could be level or edge triggered type by configuration.

2.5.2 Block Diagram

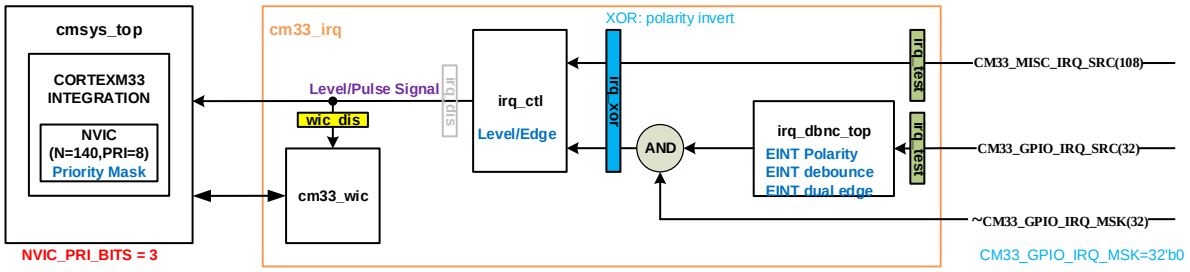


Figure 2-23 CM33_IRQ Block Diagram

2.5.3 Interrupt Table

Table 2-11 CM33 interrupt

MCU IRQ NUM	Interrupt Name	Interrupt Description	Polarity	Edge / Level	EINT
0	wic_int_wake_up	WIC wakeup interrupt to CM33	H	edge(HW) level(SW)	X
1	Reserved				
2	Reserved				
3	~wdt_irq_b0	CM33 WDT interrupt (wdt_irq_b[0])	H	edge	X
4	~uart_irq_b	CM33 UART interrupt	H	level	X
5	infra_bus_int	Infra bus error interrupt	H	level	X
6	dbgsys_CDBGPWRUPREQ	CoreSight debug power up req	H	level	X
7	dbgsys_CDBGPWRUPACK	CoreSight debug power up ack	H	level	X
8	~wdt_irq_b1	CM33 WDT interrupt (wdt_irq_b[1])	H	level	X
9	Reserved				
10	~apxgpt_irq_b0[0]	GPT_32_0	H	level	X
11	~apxgpt_irq_b0[1]	GPT_32_1	H	level	X
12	~apxgpt_irq_b0[2]	GPT_32_2	H	level	X
13	~apxgpt_irq_b0[3]	GPT_32_3	H	level	X
14	~apxgpt_irq_b0[4]	GPT_32_4	H	level	X
15	~apxgpt_irq_b0[5]	GPT_64	H	level	X
16	~devapc_INFRA_AON_secure_vio_irq_b	devapc secure violate	H	level	X
17	~devapc_AUD_BUS_PDN_secure_vio_irq_b	AUDIO_BUS devapc secure violate	H	level	X
18	conn_ap_bus_req_rise_irq	conn_ap_bus_req rising edge IRQ	H	level	X
19	conn_ap_bus_req_fall_irq	conn_ap_bus_req falling edge IRQ	H	level	X
20	conn_apsrc_req_rise_irq	conn_apsrc_req rising edge IRQ	H	level	X
21	conn_apsrc_req_fall_irq	conn_apsrc_req falling edge IRQ	H	level	X
22	conn_ap_bus_req_high_irq	conn_ap_bus_req level high IRQ	H	level	X
23	conn_ap_bus_req_low_irq	conn_ap_bus_req level low IRQ	H	level	X
24	conn_apsrc_req_high_irq	conn_apsrc_req level high IRQ	H	level	X
25	conn_apsrc_req_low_irq	conn_apsrc_req level low IRQ	H	level	X
26	infra_bus_timeout_irq	infra bus timeout IRQ	H	level	X

MCU IRQ NUM	Interrupt Name	Interrupt Description	Polarity	Edge / Level	EINT
27	cm33_local_bus_int	CM33 local bus interrupt	H	level	X
28	Reserved				
29	Reserved				
30	Reserved				
31	Reserved				
32	Reserved				
33	~top_uart0_irq_b	TOP UART	H	level	X
34	~top_uart1_irq_b	TOP UART	H	level	X
35	~i2c0_irqb	I2C transfer done or error	H	level	X
36	~i2c1_irqb	I2C transfer done or error	H	level	X
37	~sdctl_top_fw_irq_b	SDIO slave interrupt	H	level	X
38	~sdctl_top_fw_irq_b_qout	SDIO slave interrupt	H	level	X
39	~spi_irq_b	SPI master transfer done or pause	H	level	X
40	~spi_irq_b	SPI master transfer done or pause	H	level	X
41	Reserved				
42	Reserved				
43	~irrx_irq_b	IRRX decoding done	H	level	X
44	Reserved				
45	Reserved				
46	Reserved				
47	Reserved				
48	Reserved				
49	Reserved				
50	Reserved				
51	~audio_irq_mcu_b	AFE interrupt	H	level	X
52	Reserved				
53	sysram_top_int	SYSRAM out-of-bound access error	H	level	X
54	~mpu_irq_b_l2_pwr	illegal accesses to asic_mpu instances in L2	H	level	X
55	~mpu_irq_b_psram_pwr	illegal accesses to asic_mpu for PSRAM	H	level	X
56	~cq_dma_irq_b[0]	CQ_DMA Channel 0 finishes operation	H	level	X

MCU IRQ NUM	Interrupt Name	Interrupt Description	Polarity	Edge / Level	EINT
57	~cq_dma_irq_b[1]	CQ_DMA Channel 1 finishes operation	H	level	X
58	~cq_dma_irq_b[2]	CQ_DMA Channel 2 finishes operation	H	level	X
59	~msdc_irq_b_0p	normal IRQ	H	level	X
60	~msdc_wakeup_ps_0p	wakeup IRQ	H	level	X
61	Reserved				
62	Reserved				
63	~ap_dma_irq_b[0]	AP_DMA Channel 0 (I2C 0) finishes operation	H	level	X
64	~ap_dma_irq_b[1]	AP_DMA Channel 1 (I2C 1) finishes operation	H	level	X
65	~ap_dma_irq_b[2]	AP_DMA Channel 2 (Reserved) finishes operation	H	level	X
66	~ap_dma_irq_b[3]	AP_DMA Channel 3 (Reserved) finishes operation	H	level	X
67	~ap_dma_irq_b[4]	AP_DMA Channel 4 (UART 0 TX) finishes operation	H	level	X
68	~ap_dma_irq_b[5]	AP_DMA Channel 5 (UART 0 RX) finishes operation	H	level	X
69	~ap_dma_irq_b[6]	AP_DMA Channel 6 (UART 1 TX) finishes operation	H	level	X
70	~ap_dma_irq_b[7]	AP_DMA Channel 7 (UART 1 RX) finishes operation	H	level	X
71	~ap_dma_irq_b[8]	AP_DMA Channel 8 (BTIF TX) finishes operation	H	level	X
72	~ap_dma_irq_b[9]	AP_DMA Channel 9 (BTIF RX) finishes operation	H	level	X
73	~ap_dma_irq_b[10]	AP_DMA Channel 10 (Reserved) finishes operation	H	level	X
74	~ap_dma_irq_b[11]	AP_DMA Channel 11 (AUXADC RX) finishes operation	H	level	X
75	~btif_host_irq_b	BTIF host interrupt	H	level	X
76	~flash_int_b	Flash Controller Interrupt	H	level	X
77	~conn2ap_wfdma_irq_b	Wi-Fi host interrupt	H	level	X
78	~bgf2ap_wdt_irq_b	bgf WDT interrupt	H	edge	X
79	~bgf2ap_btif0_wakeup_out_b	bgf BTIF wakeup interrupt	H	level	X

MCU IRQ NUM	Interrupt Name	Interrupt Description	Polarity	Edge / Level	EINT
80	~conn2ap_sw_irq_b	bgf software interrupt for debug	H	level	X
81	~bt2ap_isoch_irq_b	bt iso channel interrupt	H	level	X
82	~bt_cvsd_int_b	bt CVSD interrupt	H	level	X
83	~ccif_wf2ap_sw_irq_b	wf software interrupt for debug from ccif trigger	H	level	X
84	~ccif_bgf2ap_sw_irq_b	bgf software interrupt for debug from ccif trigger	H	level	X
85	~wm_conn2ap_wdt_irq_b		H	edge	X
86	~sema_release_inform_m2_int_b	semaphore release IRQ for m2	H	level	X
87	~sema_release_inform_m3_int_b	semaphore release IRQ for m3	H	level	X
88	~sema_m2_timeout_int_b	semaphore timeout IRQ for m2	H	level	X
89	~sema_m3_timeout_int_b	semaphore timeout IRQ for m3	H	level	X
90	~conn_bgf_hif_on_host_int_b				
91	Reserved				
92	Reserved				
93	~wf2ap_sw_irq_b	wf2ap software IRQ	H	level	X
94	cq_dma_sec_abort	CQ_DMA APB secure violation happens	H	level	X
95	ap_dma_sec_abort	AP_DMA APB secure violation happens	H	level	X
96	~sdio_sdio_cmd_i	SDIO slave wakeup interrupt	H	edge	X
97	Reserved				
98	~adc_comp_irq_b	ADC comparator IRQ	H	level	X
99	~adc_fifo_int_b	ADC FIFO mode interrupt	H	level	X
100	~gcpu_irq_b	GCPU interrupt	H	level	X
101	~ecc_irq_b	ECC interrupt	H	level	X
102	~trng_irq_b	TRNG interrupt	H	level	X
103	~sej_apxgpt_irq_b	SEJ GPT interrupt	H	level	X
104	~sej_wdt_irq_b	SEJ WDT interrupt	H	level	X
105	Reserved				
106	Reserved				
107	Reserved				
108	gpio_irq[0]	GPIO IRQ	H	configurable	V
109	gpio_irq[1] / sdio_sdio_cmd_i	GPIO IRQ / sdio_sdio_cmd_i	H	configurable	V

MCU IRQ NUM	Interrupt Name	Interrupt Description	Polarity	Edge / Level	EINT
110	gpio_irq[2]	GPIO IRQ	H	configurable	V
111	gpio_irq[3]	GPIO IRQ	H	configurable	V
112	gpio_irq[4]	GPIO IRQ	H	configurable	V
113	gpio_irq[5]	GPIO IRQ	H	configurable	V
114	gpio_irq[6]	GPIO IRQ	H	configurable	V
115	gpio_irq[7]	GPIO IRQ	H	configurable	V
116	gpio_irq[8]	GPIO IRQ	H	configurable	V
117	gpio_irq[9]	GPIO IRQ	H	configurable	V
118	gpio_irq[10]	GPIO IRQ	H	configurable	V
119	gpio_irq[11]	GPIO IRQ	H	configurable	V
120	gpio_irq[12]	GPIO IRQ	H	configurable	V
121	gpio_irq[13]	GPIO IRQ	H	configurable	V
122	gpio_irq[14]	GPIO IRQ	H	configurable	V
123	gpio_irq[15]	GPIO IRQ	H	configurable	V
124	gpio_irq[16]	GPIO IRQ	H	configurable	V
125	Reserved				
126	gpio_irq[18]	GPIO IRQ	H	configurable	V
127	Reserved				
128	Reserved				
129	Reserved				
130	Reserved				
131	Reserved				

MCU IRQ NUM	Interrupt Name	Interrupt Description	Polarity	Edge / Level	EINT
132	Reserved				
133	Reserved				
134	Reserved				
135	Reserved				
136	Reserved				
137	gpio_irq[29]	GPIO IRQ	H	configurable	V
138	~sdio_sdio_cmd_i	~sdio_sdio_cmd_i	H	configurable	V
139	~cm33_pad_uart_rx / ~sdio_sdio_cmd_i	~cm33_pad_uart_rx / ~sdio_sdio_cmd_i	H	configurable	V

3 Radio Characteristics

3.1 Wi-Fi Radio Characteristics

3.1.1 Wi-Fi RF Block Diagram

Figure 3-1 illustrates the Wi-Fi RF function block. The MT7931AN integrates LNA, PA, and TRSW.
The frond-end loss with diplexer: The insertion loss for 2.4 GHz band is 1.5 dB, while the insertion loss for 5 GHz band is 2 dB.

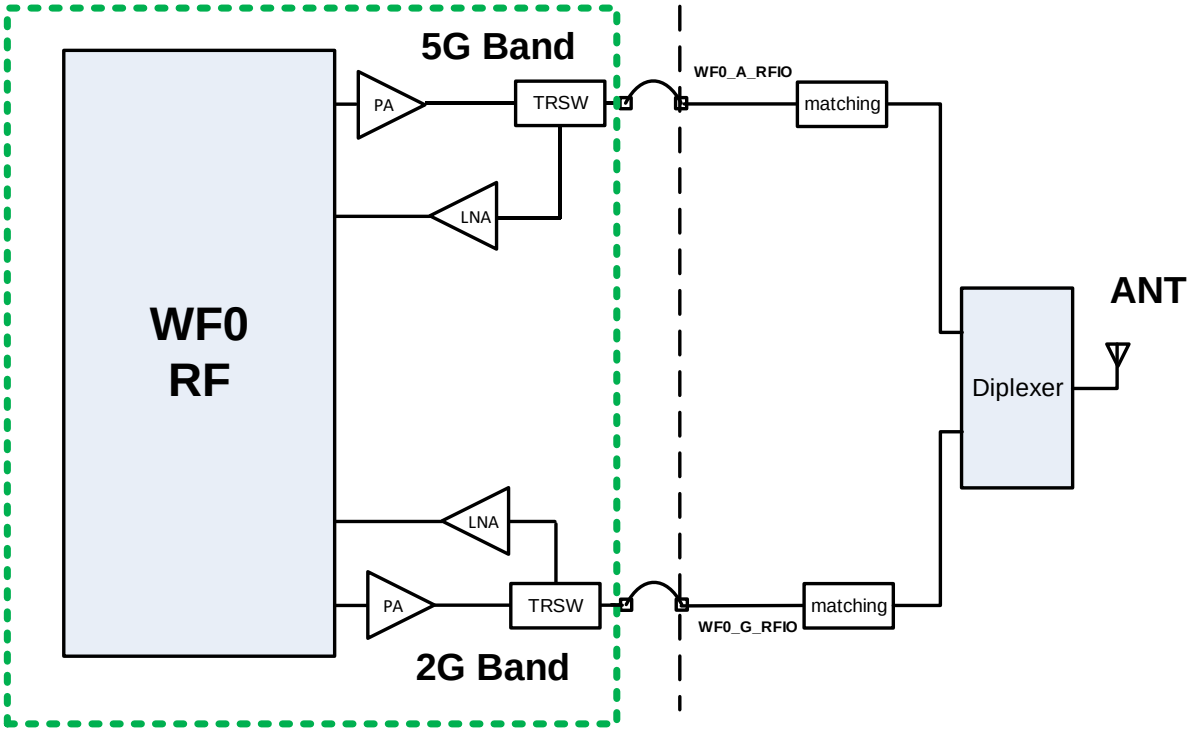


Figure 3-1 Wi-Fi RF block diagram

3.1.2 Wi-Fi RF 2.4G Band Receiver Specifications

The specifications listed in the table below are measured at the antenna port with the front-end loss.

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		2412	-	2484	MHz
RX sensitivity	1 Mbps CCK	-	-96.5	-	dBm
	2 Mbps CCK	-	-93	-	dBm
	5.5 Mbps CCK	-	-91	-	dBm
	11 Mbps CCK	-	-88	-	dBm

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
RX sensitivity	6 Mbps OFDM	-	-93.5	-	dBm
	9 Mbps OFDM	-	-91	-	dBm
	12 Mbps OFDM	-	-90.5	-	dBm
	18 Mbps OFDM	-	-88	-	dBm
	24 Mbps OFDM	-	-84.5	-	dBm
	36 Mbps OFDM	-	-81.5	-	dBm
	48 Mbps OFDM	-	-77	-	dBm
	54 Mbps OFDM	-	-75.5	-	dBm
RX Sensitivity BW=20 MHz Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-92.5	-	dBm
	MCS 1	-	-89	-	dBm
	MCS 2	-	-87	-	dBm
	MCS 3	-	-84	-	dBm
	MCS 4	-	-80.5	-	dBm
	MCS 5	-	-76	-	dBm
	MCS 6	-	-75	-	dBm
	MCS 7	-	-73.5	-	dBm
RX Sensitivity VHT20 BCC	MCS 0		-92.5		dBm
	MCS 1		-89		dBm
	MCS 2		-87		dBm
	MCS 3		-84		dBm
	MCS 4		-80.5		dBm
	MCS 5		-76		dBm
	MCS 6		-75		dBm
	MCS 7		-73.5		dBm
	MCS 8		-69		dBm
RX Sensitivity HE20 BCC (4 x LTF)	MCS0	-	-92	-	dBm
	MCS1	-	-88.5	-	dBm
	MCS2	-	-86	-	dBm
	MCS3	-	-83	-	dBm
	MCS4	-	-80	-	dBm
	MCS5	-	-75.5	-	dBm
	MCS6	-	-74	-	dBm
	MCS7	-	-72.5	-	dBm
	MCS8	-	-68.5	-	dBm
Maximum Receive Level	11 Mbps CCK	-	-10	-	dBm
	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
Receive Adjacent Channel Rejection	1 Mbps CCK	-	43	-	dBm
	11 Mbps CCK	-	41	-	dBm
	6 Mbps OFDM	-	41	-	dBm
	54 Mbps OFDM	-	25	-	dBm
Receive Adjacent Channel Rejection	MCS 0	-	36	-	dBm
	MCS 7	-	13	-	dBm

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
(HT20)					

Sensitivity level at 25°C and 3.3V

3.1.3 Wi-Fi RF 2.4G Band Transmitter Specifications

The specifications in the table below are measured at the antenna port with the frond-end loss.

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		2412	-	2484	MHz
Output power at 25°C and 3.3V with mask and EVM compliance	1~11 Mbps CCK	-	21.5	-	dBm
	6 Mbps OFDM	-	20.5	-	dBm
	54 Mbps OFDM	-	18	-	dBm
	HT20, MCS 0	-	19.5	-	dBm
	HT20, MCS 7	-	17.5	-	dBm
	VHT20, MCS 0	-	19.5	-	dBm
	VHT20, MCS 8	-	16.5	-	dBm
	HE20, MCS 0	-	19.5	-	dBm
	HE20, MCS 8	-	16.5	-	dBm
Output power variation[1]	TSSI closed-loop control across all temperature range and channels and VSWR ≦ 1.5:1.	-2		2	dB
Carrier suppression		-		-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-	dBm/MHz
	3nd Harmonic	-	-45	-	dBm/MHz

Note 1: VDD33 is within ±5% of typical value

3.1.4 Wi-Fi RF 5G Band Receiver Specifications

The specifications listed in the table below are measured at the antenna port with the front-end loss.

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		5180	-	5825	MHz
RX sensitivity	6 Mbps OFDM	-	-93	-	dBm
	9 Mbps OFDM	-	-90.5	-	dBm
	12 Mbps OFDM	-	-90	-	dBm
	18 Mbps OFDM	-	-87.5	-	dBm
	24 Mbps OFDM	-	-84	-	dBm
	36 Mbps OFDM	-	-81	-	dBm

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
	48 Mbps OFDM	-	-76.5	-	dBm
	54 Mbps OFDM	-	-75	-	dBm
RX Sensitivity BW=20 MHz VHT Mixed Mode 800ns Guard Interval Non-STBC	MCS 0	-	-92	-	dBm
	MCS 1	-	-88.5	-	dBm
	MCS 2	-	-86.5	-	dBm
	MCS 3	-	-83.5	-	dBm
	MCS 4	-	-80	-	dBm
	MCS 5	-	-75.5	-	dBm
	MCS 6	-	-74.5	-	dBm
	MCS 7	-	-73	-	dBm
	MCS 8	-	-68.5	-	dBm
RX Sensitivity HE20 BCC (4 x LTF)	MCS 0	-	-91.5	-	dBm
	MCS 1	-	-88	-	dBm
	MCS 2	-	-85.5	-	dBm
	MCS 3	-	-82.5	-	dBm
	MCS 4	-	-79.5	-	dBm
	MCS 5	-	-75	-	dBm
	MCS 6	-	-73.5	-	dBm
	MCS 7	-	-72	-	dBm
	MCS 8	-	-68	-	dBm
Maximum Receive Level	6 Mbps OFDM	-	-10	-	dBm
	54 Mbps OFDM	-	-10	-	dBm
	MCS0	-	-10	-	dBm
	MCS7	-	-10	-	dBm
Receive Adjacent Channel Rejection (VHT20)	MCS0	-	27	-	dBm
	MCS8	-	0	-	dBm

Sensitivity level at 25°C and 3.3V

3.1.5 Wi-Fi RF 5G Band Transmitter Specifications

Parameter	Description	Performance			
		Min.	Typ.	Max.	Unit
Frequency range		5180	-	5825	MHz
Output power at 25°C and 3.3V with mask and EVM compliance	6 Mbps OFDM	-	21	-	dBm
	54 Mbps OFDM	-	18.5	-	dBm
	HT20, MCS 0	-	20	-	dBm
	HT20, MCS 7	-	17.5	-	dBm
	HE20, MCS8	-	16.5	-	dBm
Output power variation[1]	TSSI closed-loop control across all temperature range and channels and VSWR ≦1.5:1.	-2		2	dB
Carrier suppression		-		-30	dBc
Harmonic Output Power	2nd Harmonic	-	-45	-	dBm/MHz
	3nd Harmonic	-	-45	-	dBm/MHz

3.2 Bluetooth Radio Characteristics

3.2.1 Bluetooth RF Block Diagram

Figure 3-2 illustrates the Bluetooth RF function block. The MT7931AN integrates LNA, PA, and TRSW. The frond-end losses are both 0.2 dB.

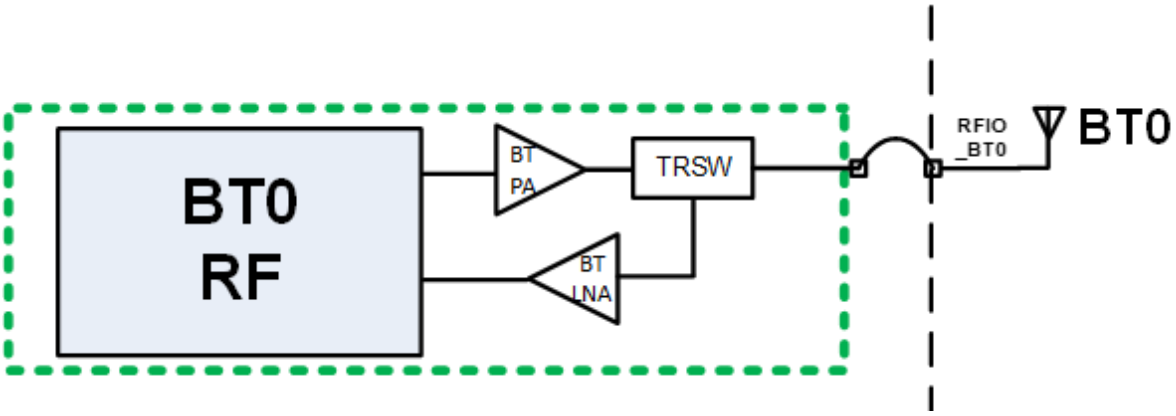


Figure 3-2 Bluetooth RF block diagram

3.2.2 Bluetooth LE un-coded PHY Receiver Specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description	Min.	Typ.	Max.	Unit
Channel Frequency Coverage		2402	-	2480	MHz
Receiver Sensitivity (*)	BLE 1Mbps(PER < 30.8%)	-	-97	-	dBm
	BLE 2Mbps(PER < 30.8%)	-	-94	-	
Max. Usable Signal	BLE 1Mbps(PER < 30.8%)	-10	-	-	dBm
	BLE 2Mbps(PER < 30.8%)	-10	-	-	dBm
C/I Co-channel	BLE 1Mbps(PER < 30.8%)	-	9	21	dB
C/I 1MHz		-	-3	15	dB
C/I 2MHz		-	-30	-17	dB
C/I ≧3MHz		-	-33	-27	dB
C/I Image channel		-	-20	-9	dB
C/I Image 1MHz		-	-30	-15	dB
C/I Co-channel	BLE 2Mbps(PER < 30.8%)	-	7	21	dB
C/I 1MHz		-	-3	15	dB
C/I 2MHz		-	-27	-17	dB
C/I ≧3MHz		-	-30	-27	dB
C/I Image channel		-	-17	-9	dB
C/I Image 1MHz		-	-27	-15	dB
Out-of-band Blocking	30MHz to 2000MHz	-30	-	-	dBm
	2001MHz to 2339MHz	-35	-	-	dBm
	2501MHz to 3000MHz	-35	-	-	dBm
	3001MHz to 12.75GHz	-30	-	-	dBm

Note 1: The receiver sensitivity is measured at the BT antenna port.

3.2.3 Bluetooth LE Un-Coded PHY Transmitter Specifications

The specifications in table below are measured at the antenna port with the frond-end loss.

Parameter	Description		Min.	Typ.	Max.	Unit
Channel frequency coverage			2402	-	2480	MHz
Output Power (*)	BLE 1Mbps		-	9.5	-	dBm
	BLE 2Mbps		-	9.5	-	
Carrier Frequency Offset and Drift	Frequency offset	BLE 1Mbps	-150	±10	150	kHz
		BLE 2Mbps	-150	±10	150	
	Frequency drift	BLE 1Mbps	-50	±10	50	kHz
		BLE 2Mbps	-50	±10	50	
	Max. drift rate	BLE 1Mbps	-20	±10	20	KHz/50us
		BLE 2Mbps	-20	±10	20	
Modulation Characteristic	$\triangle f1_{avg}$	BLE 1Mbps	225	250	275	kHz
		BLE 2Mbps	450	500	550	
	$\triangle f2_{max}$ (For at least 99% of all $\triangle f2_{max}$)	BLE 1Mbps	185	-	-	kHz
		BLE 2Mbps	370	-	-	
	$\triangle f2_{avg}/\triangle f1_{avg}$	BLE 1Mbps	0.8	0.9	-	
		BLE 2Mbps	0.8	0.9	-	
In-band Spurious Emission	±2MHz offset	BLE 1Mbps	-	-35	-20	dBm
	±4MHz,±5MHz offset	BLE 2Mbps	-	-35	-20	
	>±3MHz offset	BLE 1Mbps	-	-40	-30	dBm

Note 1: The output power is measured at the antenna port.

3.2.4 Bluetooth LE Coded PHY Receiver Specifications

Parameter	Description	Min.	Typ.	Max.	Unit
Channel frequency coverage		2402	-	2480	MHz
Receiver sensitivity (*)	BLE 500Kbps (PER < 30.8%)	-	-98	-	dBm
	BLE 125Kbps (PER < 30.8%)	-	-103	-	
C/I co-channel	BLE 500Kbps (PER < 30.8%)	-	5	17	dB
	BLE 125Kbps (PER < 30.8%)	-	6	12	
C/I 1MHz	BLE 500Kbps (PER < 30.8%)	-	-8	11	dB
	BLE 125Kbps (PER < 30.8%)	-	-12	6	
C/I 2MHz	BLE 500Kbps (PER < 30.8%)	-	-34	-21	dB
	BLE 125Kbps (PER < 30.8%)	-	-39	-26	
C/I ≧3MHz	BLE 500Kbps (PER < 30.8%)	-	-37	-31	dB
	BLE 125Kbps (PER < 30.8%)	-	-42	-36	
C/I image channel	BLE 500Kbps (PER < 30.8%)	-	-24	-13	dB
	BLE 125Kbps (PER < 30.8%)	-	-29	-18	
C/I Image 1MHz	BLE 500Kbps (PER < 30.8%)	-	-34	-19	dB
	BLE 125Kbps (PER < 30.8%)	-	-39	-24	

Note 1: The receiver sensitivity is measured at the BT antenna port.

3.2.5 Bluetooth LE Coded PHY Transmitter Specifications

The specification in table below is measured at the antenna port, which includes the frond-end loss.

Parameter	Description		Min.	Typ.	Max.	Unit
Channel frequency coverage			2402	-	2480	MHz
Output power(*)	BLE 500Kbps		-	9.5	-	dBm
	BLE 125Kbps		-	9.5	-	
Carrier frequency offset and drift	Frequency offset	BLE 125Kbps	-150	±10	150	kHz
	Frequency drift	BLE 125Kbps	-50	±10	50	kHz
	Max. drift rate	BLE 125Kbps	-19.2	±10	19.2	KHz/48us
Modulation characteristic	$\triangle f1_{avg}$	BLE 125Kbps	225	250	275	kHz
	△f1max (For at least 99% of all △f1max)	BLE 125Kbps	185	245	-	kHz

Note 1: The output power is measured at the BT antenna port.

4 Electrical Characteristics

4.1 Absolute Maximum Rating

Table 4-1 Absolute maximum rating

Symbol	Parameters	Maximum rating	Unit
VDD33	3.3V Supply Voltage	-0.3 to 3.63	V
T_{STG}	Storage Temperature	-40 to +125	°C
VESD	ESD protection (HBM)	1000	V

4.2 Recommended Operating Range

Table 4-2 Recommended operating range

Symbol	Rating	Min.	Typ.	Max.	Unit
VDD33	3.3V Supply Voltage	2.97	3.3	3.63	V
$T_{JUNCTION}$	Junction Temperature	-30	-	125	°C

4.3 DC Characteristics

Table 4-3 DC characteristics

Symbol	Parameter	Conditions	Min.	Max.	Unit
V_{IL}	Input Low Voltage	LVTTL	-0.3	0.25*VDD33	V
V_{IH}	Input High Voltage		0.625*VDD33	VDD33+0.3	V
V_{OL}	Output Low Voltage	$\|I_{OL}\|$ = 2~8 mA	-0.3	0.45	V
V_{OH}	Output High Voltage	$\|I_{OH}\|$ = 2~8 mA	VDD33-0.45	VDD33+0.3	V
R_{PU0}	Input Pull-Up Resistance	PUPD=low, R0=high, R1=low	5	10	kΩ
R_{PD0}	Input Pull-Down Resistance	PUPD=high, R0=high, R1=low	5	10	kΩ
R_{PU1}	Input Pull-Up Resistance	PUPD=low, R0=low, R1=high	10	100	kΩ
R_{PD1}	Input Pull-Down Resistance	PUPD=high, R0=low, R1=high	10	100	kΩ

4.4 XTAL Oscillator

The table below lists the requirement for the XTAL.

Table 4-4 XTAL oscillator requirement

Parameter	Value
Frequency	26MHz
Frequency stability over operating temperature range	±10 ppm (referred to the value at 25°C)
Aging	±3 ppm/year

4.5 PMU Characteristics

Table 4-5 PMU electrical characteristics

PARAMETER	CONDITIONS	PERFORMANCE			
		Min.	Typ.	Max.	UNIT
BUCK-R (Switching regulator)					
Input voltage		2.97	3.3	3.63	V
Output voltage		1.14	1.2	1.32	V
Output current		-	-	550	mA
Quiescent current		-	150	180	uA
Efficiency	100~200mA load current	84	87	-	%
Over-current Shutdown		1	1.3	1.6	A
BUCK-D (Switching regulator)					
Input voltage		2.97	3.3	3.63	V
Output voltage		0.62	0.7	0.85	V
Output current		-	-	740	mA
Quiescent current		-	150	180	uA
Efficiency	10~200mA load current	79	82	-	%
Over-current Shutdown		1.3	1.7	2.1	A
PHYLDO					
Input voltage		2.97	3.3	3.63	V
Output voltage		1.62	1.8	1.98	V
Output current		-	-	150	mA
Quiescent current		-	10	20	uA
ALDO					
Input voltage		2.97	3.3	3.63	V

PARAMETER	CONDITIONS	PERFORMANCE			
		Min.	Typ.	Max.	UNIT
Output voltage		1.62	1.8	1.98	V
Output current		-	-	150	mA
Quiescent current		-	10	20	uA
AUXLDO					
Input voltage		2.97	3.3	3.63	V
Output voltage		1.62	1.8	1.98	V
Output current		-	-	1	mA
Quiescent current		-	10	20	uA
MLDO					
Input voltage		1.14	1.2	1.26	V
Output voltage		0.62	0.8	0.88	V
Output current		-	-	120	mA
Quiescent current		-	10	20	uA
General					
AVDD33 UVLO rising threshold		-	2.85	-	V
AVDD33 UVLO falling threshold		-	2.7	-	V
PMU_EN high threshold		1.09	1.2	1.31	V
PMU_EN low threshold		0.8	0.9	1	V
Thermal shutdown			150		°C

4.6 Auxiliary ADC Characteristics

This section specifies the electrical characteristics of the auxiliary ADC.

Table 4-6 ADC specification

Symbol	Parameter	Min.	Typ.	Max.	Unit	
N	Resolution		12		Bit	
CH	Channel Number		12		Channel	12 AGPIOs in digital part
FC	Clock Rate	1	2	6	MHz	
FS	Sampling Rate @ N-Bit	1	2	6	MSPS	FS=2MHz default
TS	Sample period	0.17	0.5	1	µS	=1/FS
VPP	Input Swing			1	V	
VIN	Input voltage	0		1	V	
SC	Sampling capacitance		2.048		pF	

Symbol	Parameter	Min.	Typ.	Max.	Unit	
RIN	Series Input Impedance: Unselected channel Selected channel			400M 10K	Ohm	
	Dither waveform type		Sawtooth			
	Dither step size (programmable)	0	4	4	LSB	Programmable (0,4)
N_{avg}	Number of samples averaged in hardware (programmable)	1	32	64		Programmable (1,2,4, 8,16, 32,64)
T_{dither}	Dither period	1	16	16	TS	Programmable(1,2,4,8,16)
	Dither Magnitude	0	64	64	LSB	=DITHERSTEP*T_{dither}
DNL	Differential Nonlinearity without dithering and averaging		± 1	± 2	LSB	No dither and no averaging
INL	Integral Nonlinearity without dithering and averaging		± 2	± 4	LSB	
$DNL_{dither+average}$	Differential Nonlinearity with dithering and averaging		± 0.5	± 1	LSB	With dither and averaging
$INL_{dither+average}$	Integral Nonlinearity with dithering and averaging			± 4	LSB	
OE	Offset Error			± 10	mV	
FSE	Full Swing Error			± 50	mV	
SNR	Signal to Noise Ratio	55	58	61	dB	@ 1kHz input frequency
DVDD	Digital Power Supply	0.54	0.8	0.88	V	Have VAD Mode
AVDD	Analog Power Supply	1.62	1.8	1.98	V	
IOVDD	IO Power Supply	1.62	1.8	1.98	V	
T	Operating Temperature	-40		125	℃	
	Current Consumption			400	μA	
	Power-Down Current			1	μA	

4.7 Thermal Characteristics

Θ_{JC} assumes that all the heat is dissipated through the top of the package, while Ψ_{Jt} assumes that the heat is dissipated through the top, sides, and the bottom of the package. Thus it's suggested to use Ψ_{Jt} to estimate the junction temperature.

Symbol	Description	Performance	
		Typical	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance	30.27	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	8.20	°C/W
Ψ_{Jt}	Junction to the package thermal resistance	2.84	°C/W

Note: JEDEC 51-7 system FR4 PCB size: 76.2x114.3mm (3”x4.5”), 2 layer.

Table 4-7-1 Thermal characteristics

Symbol	Description	Performance	
		Typical	Unit
T_J	Maximum Junction Temperature (Plastic Package)	125	°C
Θ_{JA}	Junction to ambient temperature thermal resistance	20.26	°C/W
Θ_{JC}	Junction to case temperature thermal resistance	8.20	°C/W
Ψ_{Jt}	Junction to the package thermal resistance	1.00	°C/W

Note: JEDEC 51-7 system FR4 PCB size: 76.2x114.3mm (3”x4.5”), 4 layer.

Table 4-8-2 Thermal characteristics

5 Package Specification

5.1 Pin Layout

The MT7931AN uses DRQFN package, the dimension is 9mm x 8.7mm with 0.5mm pin pitch

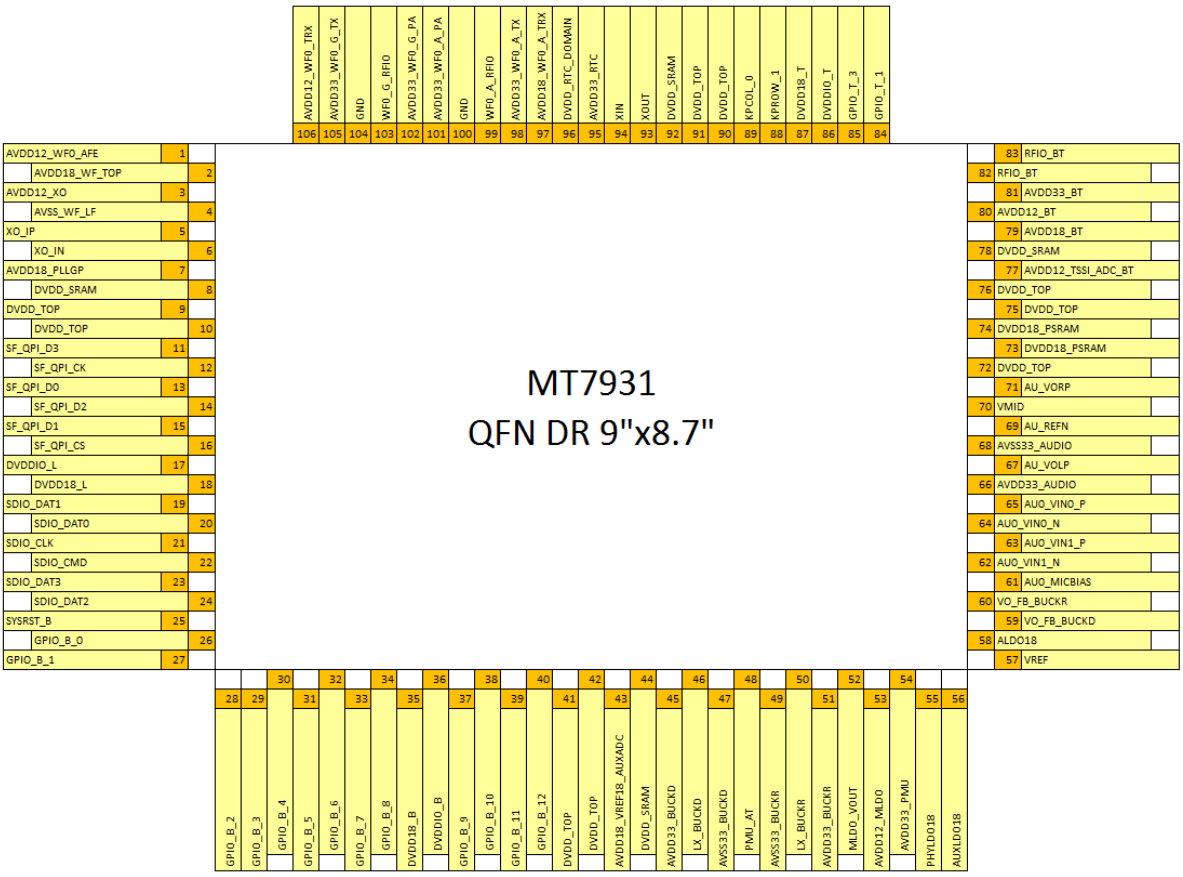


Figure 5-1 Package ball-out

5.2 Pin Description

The section describes pin functionalities of the MT7931AN chip.

Table 5-1. Pin descriptions

QFN	Pin Name	Pin Description
RESET and GPIO		
25	PAD_SYSRST_B	Chip hardware fundamental reset pin
26	PAD_GPIO_B_0	GPIO
27	PAD_GPIO_B_1	GPIO
28	PAD_GPIO_B_2	GPIO
29	PAD_GPIO_B_3	GPIO
30	PAD_GPIO_B_4	GPIO
31	PAD_GPIO_B_5	GPIO with AUXADC Channel Interface
32	PAD_GPIO_B_6	GPIO with AUXADC Channel Interface
33	PAD_GPIO_B_7	GPIO with AUXADC Channel Interface
34	PAD_GPIO_B_8	GPIO with AUXADC Channel Interface
37	PAD_GPIO_B_9	GPIO with AUXADC Channel Interface
38	PAD_GPIO_B_10	GPIO with AUXADC Channel Interface
39	PAD_GPIO_B_11	GPIO with AUXADC Channel Interface
40	PAD_GPIO_B_12	GPIO with AUXADC Channel Interface
84	PAD_GPIO_T_1	GPIO
85	PAD_GPIO_T_3	GPIO
89	PAD_KPCOL_0	GPIO with Keypad Interface
88	PAD_KPROW_1	GPIO with Keypad Interface
21	PAD_SDIO_CLK	GPIO with SDIO Interface
22	PAD_SDIO_CMD	GPIO with SDIO Interface
20	PAD_SDIO_DAT0	GPIO with SDIO Interface
19	PAD_SDIO_DAT1	GPIO with SDIO Interface
24	PAD_SDIO_DAT2	GPIO with SDIO Interface
23	PAD_SDIO_DAT3	GPIO with SDIO Interface
12	PAD_SF_QPI_CK	Flash Interface
16	PAD_SF_QPI_CS	Flash Interface
13	PAD_SF_QPI_D0	Flash Interface
15	PAD_SF_QPI_D1	Flash Interface
14	PAD_SF_QPI_D2	Flash Interface
11	PAD_SF_QPI_D3	Flash Interface
WF RF		
1	AVDD12_WF0_AFE	RF 1.2V power supply
106	AVDD12_WF0_SX_HF	RF 1.2V power supply

QFN	Pin Name	Pin Description
3	AVDD12_XO	RF 1.2V power supply
2	AVDD18_WF_TOP	RF 1.8V power supply
97	AVDD18_WF0_A_TRX	RF 1.8V power supply
101	AVDD33_WF0_A_PA	RF 3.3V power supply
98	AVDD33_WF0_A_TX	RF 3.3V power supply
102	AVDD33_WF0_G_PA	RF 3.3V power supply
105	AVDD33_WF0_G_TX	RF 3.3V power supply
4	AVSS_WF_LF	RF ground
99	PAD_WF0_A_RFIO	RF a-band RF port
103	PAD_WF0_G_RFIO	RF g-band RF port
6	PAD_XO_IN	Crystal input
5	PAD_XO_IP	Crystal input or external clock input
PLL		
7	AVDD18_PLLGP_TOP	PLL 1.8V power
AUXADC		
43	AVDD18_VREF18_AUXADC	AUXADC 1.8V power
PMU		
53	AVDD12_MLDO	MLDO 1.2V supply
45	AVDD33_BUCKD	BUCKD 3.3V supply
51	AVDD33_BUCKR	BUCKR 3.3V supply
54	AVDD33_PMU	PMU 3.3V supply
47	AVSS33_BUCKD	BUCKD power stage ground
49	AVSS33_BUCKR	BUCKR power stage ground
58	PAD_ALDO18	ALDO 1.8V output pin
56	PAD_AUXLDO18_S	AUXLDO 1.8V output pin
46	PAD_LX_BUCKD	BUCKD switch node
50	PAD_LX_BUCKR	BUCKR switch node
52	PAD_MLDO_VOUT	MLDO 0.8V output pin
55	PAD_PHYLDO18	PHYLDO 1.8V output pin
48	PAD_PMU_AT	PMU analog test pin
59	PAD_VO_FB_BUCKD	BUCKD output voltage feedback signal
60	PAD_VO_FB_BUCKR	BUCKR output voltage feedback signal
57	PAD_VREF	1.2V reference voltage
CODEC		
66	AVDD33_AUDIO	Audio Codec 3.3V power
68	AVSS33_AUDIO	Audio Codec ground
61	PAD_AU0_MICBIAS	CODEC_ADC ADC0 MICBIAS output

QFN	Pin Name	Pin Description
64	PAD_AU0_VIN1_N	CODEC_ADC ADC1 RCH N_port input
65	PAD_AU0_VIN1_P	CODEC_ADC ADC1 RCH P_port input
62	PAD_AU0_VIN0_N	CODEC_ADC ADC0 LCH N_port input
63	PAD_AU0_VIN0_P	CODEC_ADC ADC0 LCH P_port input
69	PAD_AU_REFN	CODEC clean ground
67	PAD_AU_VOLP	CODEC_DAC Left_chanel P_port output signal
71	PAD_AU_VORP	CODEC_DAC Right_chanel P_port output signal
70	PAD_VMID	CODEC_DAC reference voltage
BT RF		
77	AVDD12_TSSI_ADC_BT	BT 1.2V power
79	AVDD18_BT	BT 1.8V power
80	AVDD12_BT	BT 1.2V power
81	AVDD33_BT	BT 3.3V power
82,83	PAD_RFIO_BT	RF BT RF port
32K Clock		
95	AVDD33_RTC	32K Clock 3.3V power
94	PAD_XIN	Crystal input Pin
93	PAD_XOUT	Crystal input Pin
96	DVDD_RTC_DOMAIN	External DVDD source for RTC domain
PSRAM power		
73,74	DVDD18_PSRAM	PSRAM 1.8V power
Digital Power		
8,44,78,92	DVDD_SRAM	Memory power
9,10,41,42,72,75,76,90,91	DVDD_TOP	Digital core power
18	DVDD18_L	Digital IO 1.8V power
35	DVDD18_B	Digital IO 1.8V power
87	DVDD18_T	Digital IO 1.8V power
36	DVDDIO_B	Digital IO power
17	DVDDIO_L	Digital IO power
86	DVDDIO_T	Digital IO power
100,104	GND	Digital ground

5.3 PinMux

The pin multiplexing can be controlled via the table shown below.

Table 5-2 Digital IO pin configuration in each pad and the corresponding pin description

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
PAD_SYSRST_B	NA	PAD_SYSRST_B			PU	Chip hardware fundamental reset pin
SDIO_CLK	0000	GPIO[6]	I/O	I	PD	GPIO 6
	0001 *	SDIO_CLK	I			SDIO Clock
	0010	MSDC0_CLK	O			MSDC Clock
	0011	SPIM0_SCK	O			SPI0 (Master) Clock
	0100	CM33_GPIO_EINT0	I			CM33 EINT0
	0101	DEBUG_0	O			Debug Signal 0
	0110	ANT_SEL0	O			Antenna Select 0
	0111	RSVD	I			RSVD
SDIO_CMD	0000	GPIO[7]	I/O	I	PU	GPIO 7
	0001 *	SDIO_CMD	I/O			SDIO CMD
	0010	MSDC0_CMD	I/O			MSDC CMD
	0011	SPIM0_CS_N	O			SPI0 (Master) Chip Select
	0100	CM33_GPIO_EINT1	I			CM33 EINT1
	0101	DEBUG_1	O			Debug Signal 1
	0110	ANT_SEL1	O			Antenna Select 1
	0111	RSVD	I			RSVD
SDIO_DAT0	0000	GPIO[8]	I/O	I	PU	GPIO 8
	0001 *	SDIO_DAT0	O			SDIO Data[0]
	0010	MSDC0_DAT0	I/O			MSDC0 Data[0]
	0011	SPIM0_MISO	I			SPI0 (Master) Input
	0100	UART0_RTS	O			UART0 RTS
	0101	DEBUG_2	O			Debug Signal 2
	0110	ANT_SEL2	O			Antenna Select 2
	0111	CM33_GPIO_EINT0	I			CM33 EINT0
SDIO_DAT1	0000	GPIO[9]	I/O	I	PU	GPIO 9
	0001 *	SDIO_DAT1	I/O			SDIO Data[1]
	0010	MSDC0_DAT1	I/O			MSDC0 Data[1]
	0011	SPIM0_MOSI	O			SPI0 (Master) Output
	0100	UART0_CTS	I			UART0 CTS
	0101	DEBUG_3	O			Debug Signal 3
	0110	ANT_SEL3	O			Antenna Select 3

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0111	CM33_GPIO_EINT1	I			CM33 EINT1
SDIO_DAT2	0000	GPIO[10]	I/O	I	PU	GPIO 10
	0001 *	SDIO_DAT2	I/O			SDIO Data[2]
	0010	MSDC0_DAT2	I/O			MSDC0 Data[2]
	0011	I2SIN_DAT0	I			I2S In Data0
	0100	UART0_RX	I			UART0 RX
	0101	DEBUG_4	O			Debug Signal 4
	0110	I2C0_SCL	O			I2C0 Clock
	0111	CM33_GPIO_EINT2	I			CM33 EINT2
SDIO_DAT3	0000	GPIO[11]	I/O	I	PU	GPIO 11
	0001 *	SDIO_DAT3	I/O			SDIO Data[3]
	0010	MSDC0_DAT3	I/O			MSDC Data[3]
	0011	I2SO_DAT0	O			I2SO Data
	0100	UART0_TX	O			UART0 TX
	0101	DEBUG_5	O			Debug Signal 5
	0110	I2C0_SDA	I/O			I2C0 Data
	0111	CM33_GPIO_EINT3	I			CM33 EINT3
GPIO_B_0	0000	GPIO[12]	I/O	O	PU	GPIO 12
	0001 *	CONN_BGF_UART0_TXD	O			BT General UART TX
	0010	MSDC0_RST	O			MSDC0 Reset
	0011	CONN_BT_TXD	O			BT Debug UART TX
	0100	WIFI_TXD	O			Wi-Fi Debug UART TX
	0101	DEBUG_6	O			Debug Signal 6
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT4	I			CM33 EINT4
GPIO_B_1	0000	GPIO[13]	I/O	I	PU	GPIO 13
	0001 *	RSVD	I			RSVD
	0010	SPIM1_SCK	O			SPIM1 (Master) Clock
	0011	I2SO_BCK	O			I2SO BCK
	0100	UART1_RX	I			UART1 RX
	0101	DEBUG_7	O			Debug Signal 7
	0110	ANT_SEL4	O			Antenna Select 4
	0111	CM33_GPIO_EINT5	I			CM33 EINT5
GPIO_B_2	0000	GPIO[14]	I/O	O	PD	GPIO 14
	0001 *	RSVD	O			RSVD
	0010	SPIM1_MOSI	O			SPI1 (Master) Output
	0011	I2SO_LRCK	O			I2SO LRCK
	0100	RSVD				RSVD
	0101	DEBUG_8	O			Debug Signal 8

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT6	I			CM33 EINT6
GPIO_B_3	0000	GPIO[15]	I/O	I	PD	GPIO 15
	0001 *	RSVD	I			RSVD
	0010	SPIM1_MISO	I			SPI1 (Master) Input
	0011	I2SO_MCK	O			I2STX MCLK
	0100	I2SIN_MCK	O			I2SRX MCK
	0101	DEBUG_9	O			Debug Signal 9
	0110	ANT_SEL6	O			Antenna Select 6
	0111	CM33_GPIO_EINT7	I			CM33 EINT7
GPIO_B_4	0000	GPIO[16]	I/O	I	PD	GPIO 16
	0001 *	RSVD	I			RSVD
	0010	SPIM1_CS_N	O			SPI1 (Master) Chip Select
	0011	IR_IN	I			IR RX Input
	0100	I2SIN_MCK	O			I2SIN MCLK
	0101	DEBUG_10	O			Debug Signal 10
	0110	ANT_SEL7	O			Antenna Select 7
	0111	CM33_GPIO_EINT8	I			CM33 EINT8
GPIO_B_5	0000	GPIO[17]	I/O	I	PU	GPIO 17
	0001 *	CONN_BGF_UART0_RXD	I			BT General UART RX
	0010	UART0_RX	I			UART0 RX
	0011	TDMIN_MCLK	I			TDMIN MCLK
	0100	DMIC_CLK0	O			DMIC CLK0
	0101	DEBUG_11	O			Debug Signal 11
	0110	ANT_SEL8	O			Antenna Select 8
	0111	CM33_GPIO_EINT9	I			CM33 EINT9
GPIO_B_6	0000	GPIO[18]	I/O	O	PU	GPIO 18
	0001 *	CONN_BT_TXD	O			BT Debug UART TX
	0010	UART0_TX	O			UART0 TX
	0011	TDMIN_BCK	I			TDMIN BCK
	0100	DMIC_DAT0	I			DMIC DAT0
	0101	UART1_RX	I			UART1 RX
	0110	IR_IN	I			IR RX Input
	0111	CM33_GPIO_EINT10	I			CM33 EINT10
GPIO_B_7	0000	GPIO[19]	I/O	O	PD	GPIO 19
	0001 *	WIFI_TXD	O			Wi-Fi Debug UART TX
	0010	UART0_RTS	O			UART0 RTS
	0011	I2C1_SDA	I/O			I2C1 Data

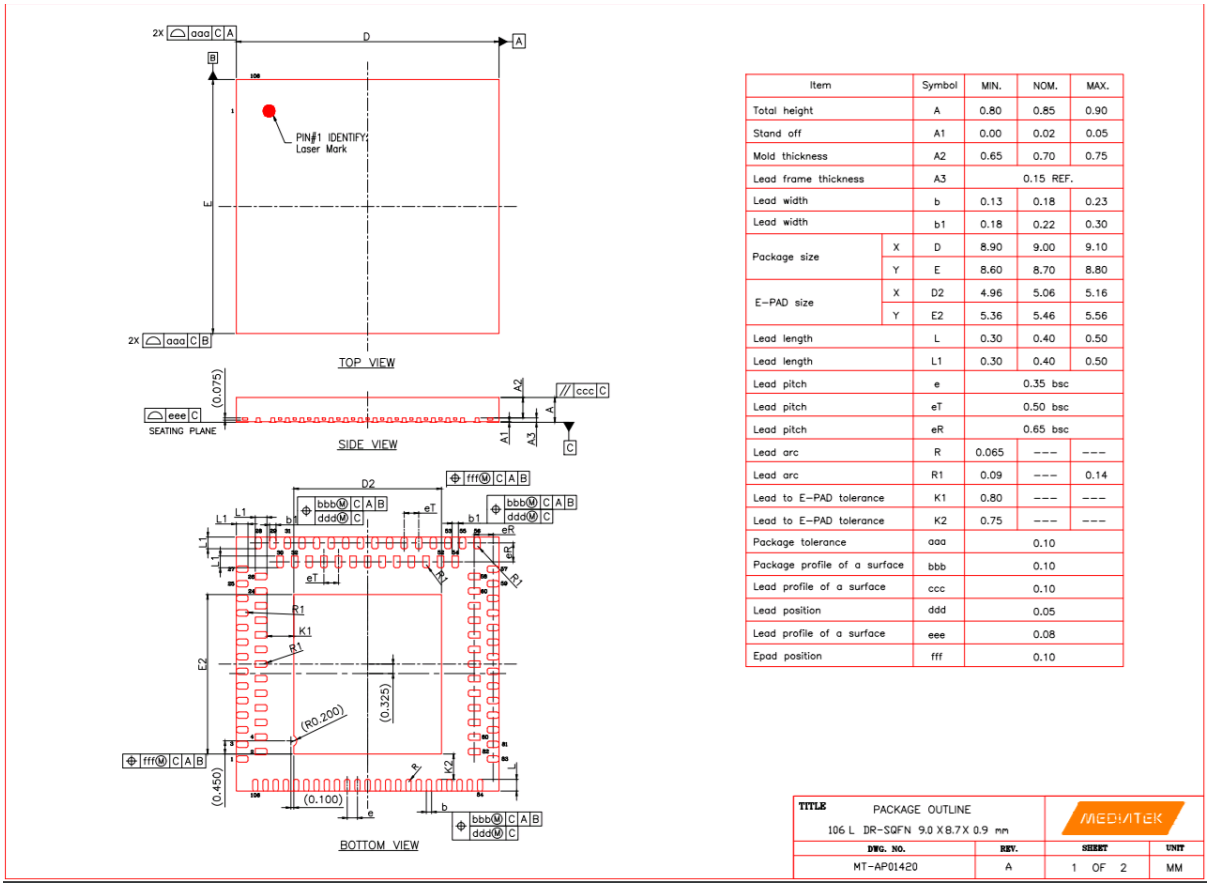
IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0100	I2SIN_LRCK	O			I2SIN LRCK
	0101	UART1_TX	O			UART1 TX
	0110	PTA_EXT_IF_FREQ	I			External PTA Frequency
	0111	CM33_GPIO_EINT11	I			CM33 EINT11
GPIO_B_8	0000	GPIO[20]	I/O	I	PD	GPIO 20
	0001 *	CONN_WF_MCU_AICE_TCKC	I			Wi-Fi N10 SWD
	0010	UART0_CTS	I			UART0 Control
	0011	I2C1_SCL	O			I2C1 Clock
	0100	I2SIN_BCK	O			I2SIN BCK
	0101	DEBUG_12	O			Debug Signal 12
	0110	PTA_EXT_IF_ACT	I			External PTA Active
	0111	CM33_GPIO_EINT12	I			CM33 EINT12
GPIO_B_9	0000	GPIO[21]	I/O	I	PU	GPIO 21
	0001 *	CONN_WF_MCU_AICE_TMSC	I/O			Wi-Fi N10 SWD
	0010	PTA_EXT_IF_PRI	I/O			External PTA Priority
	0011	TDMIN_LRCK	I/O			TDMIN LRCK
	0100	DMIC_DAT1	I			DMIC DAT1
	0101	DEBUG_13	O			Debug Signal 13
	0110	ANT_SEL9	O			Antenna Select 9
	0111	CM33_GPIO_EINT13	I			CM33 EINT13
GPIO_B_10	0000	GPIO[22]	I/O	I	PD	GPIO 22
	0001 *	CONN_BGF_MCU_AICE_TCKC	I			BT N10 SWD
	0010	PTA_EXT_IF_WLAN_ACT	O			External PTA WLAN Active
	0011	TDMIN_DI	I			TDMIN DI
	0100	DMIC_DAT2	I			DMIC Data2
	0101	DEBUG_14	O			Debug Signal 14
	0110	ANT_SEL10	O			Antenna Select 10
	0111	CM33_GPIO_EINT14	I			CM33 EINT14
GPIO_B_11	0000	GPIO[23]	I/O	I	PU	GPIO 23
	0001 *	CONN_BGF_MCU_AICE_TMSC	I/O			BT N10 SWD
	0010	DSP_URXD0	I			DSP UART RX
	0011	I2C0_SDA	I/O			I2C0 Data
	0100	DMIC_DAT3	I			DMIC Data3
	0101	DEBUG_15	O			Debug Signal 15

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0110	ANT_SEL11	O			Antenna Select 11
	0111	CM33_GPIO_EINT15	I			CM33 EINT15
GPIO_B_12	0000	GPIO[24]	I/O	O	PU	GPIO 24
	0001 *	ADSP_JTAG_TDO	O			DSP JTAG
	0010	DSP_UTXD0	O			DSP UART TX
	0011	I2C0_SCL	O			I2C0 Clock
	0100	DMIC_CLK1	O			DMIC CLK1
	0101	RSVD	O			RSVD
	0110	ANT_SEL12	O			Antenna Select 12
	0111	CM33_GPIO_EINT16	I			CM33 EINT16
GPIO_T_1	0000	GPIO[42]	I/O	I	PD	GPIO 42
	0001	RSVD	I			RSVD
	0010 *	DBSYS_SWCLK_TCLK	I			CM33_SWD (Default)
	0011	UART1_RX	I			UART1 RX
	0100	UART0_RX	I			UART0 RX
	0101	DSP_URXD0	I			DSP UART RX
	0110	ANT_SEL3	O			Antenna Select 3
	0111	CM33_GPIO_EINT1	I			CM33 EINT1
GPIO_T_3	0000	GPIO[44]	I/O	I	PD	GPIO 44
	0001	RSVD	I/O			RSVD
	0010 *	DBSYS_SWDIO_TMS	I			CM33_SWD (Default)
	0011	UART1_TX	O			UART1 TX
	0100	UART0_TX	O			UART0 TX
	0101	DSP_UTXD0	O			DSP UART TX
	0110	ANT_SEL5	O			Antenna Select 5
	0111	CM33_GPIO_EINT18	I			CM33 EINT18
KPROW_1	0000	GPIO[48]	I/O	I	PU	GPIO 48
	0001 *	CM33_UART_RX	I			CM33 UART RX (default)
	0010	RSVD	O			RSVD
	0011	KEYPAD_KPROW_1	I/O			KEYPAD_KPROW_1
	0100	DSP_URXD0	I			DSP UART RX
	0101	PWM_3	O			PWM 3
	0110	ANT_SEL9	O			Antenna Select 9
	0111	AUDIO_DEBUG_IN_0	I			AUDIO_DEBUG_IN_0
KPCOL_0	0000	GPIO[50]	I/O	O	PU	GPIO 50
	0001 *	CM33_UART_TX	O			CM33 UART TX (default)
	0010	RSVD	O			RSVD
	0011	KEYPAD_KPCOL_0	I			KEYPAD_KPCOL_0
	0100	DSP_UTXD0	O			DSP UART TX

IO Name	CR Value Default*	Name	Dir	Default		Description
				Dir	PU/PD	
	0101	PWM_5	O			PWM 5
	0110	ANT_SEL11	O			Antenna Select 11
	0111	AUDIO_DEBUG_IN_2	I			AUDIO_DEBUG_IN_2

5.4 Package Information

The package type of the MT7931AN is DR-QFN 9mm x 8.7mm and the package diagram is shown below.



Item		Symbol	MIN.	NOM.	MAX.
Total height		A	0.80	0.85	0.90
Stand off		A1	0.00	0.02	0.05
Mold thickness		A2	0.65	0.70	0.75
Lead frame thickness		A3		0.15 REF.	
Lead width		b	0.13	0.18	0.23
Lead width		b1	0.18	0.22	0.30
Package size	X	D	8.90	9.00	9.10
	Y	E	8.60	8.70	8.80
E-PAD size	X	D2	4.96	5.06	5.16
	Y	E2	5.36	5.46	5.56
Lead length		L	0.30	0.40	0.50
Lead length		L1	0.30	0.40	0.50
Lead pitch		e		0.35 bsc	
Lead pitch		eT		0.50 bsc	
Lead pitch		eR		0.65 bsc	
Lead arc		R	0.065	---	---
Lead arc		R1	0.09	---	0.14
Lead to E-PAD tolerance		K1	0.80	---	---
Lead to E-PAD tolerance		K2	0.75	---	---
Package tolerance		aaa		0.10	
Package profile of a surface		bbb		0.10	
Lead profile of a surface		ccc		0.10	
Lead position		ddd		0.05	
Lead profile of a surface		eee		0.08	
Epad position		fff		0.10	

TITLE: PACKAGE OUTLINE 106 L DR-SQFN 9.0 X 8.7 X 0.9 mm

DWG. NO.	REV.	SHEET	UNIT
MT-AP01420	A	1 OF 2	MM

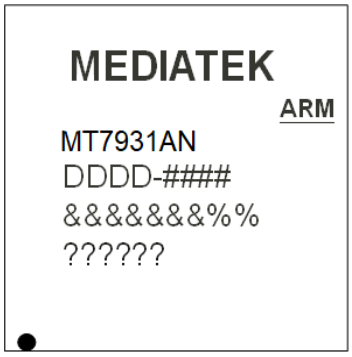
Figure 5-2. Package outline drawing

5.5 Order Information

Table 5-3 Order information

Part Number	Package
MT7931AN	9mm x 8.7mm x 0.7mm DR-QFN

5.6 Top Marking



->MT7931AN: Part number
->DDDD: Date code ####: Internal control code
->&&&&&&&: Main die Lot Number %%: Main die wafer ID
->??????: KGD lot ID

Figure 5-3 Top marking

Exhibit 1 Terms and Conditions

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