MT7663BUN Datasheet Brief

802.11a/b/g/n/ac Wi-Fi 2T2R + Bluetooth v5.1 Combo Chip

Version: 1.3
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"The full datasheet is available with an NDA"

Specifications are subject to change without notice.

Document Revision History

Revision	Date	Author	Description
1.3	2023-7-20	CH Hung	Formal release

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Lists of Tables and Figures

1 System overview

1.1 General Description

MT7663BUN is highly integrated single chip which features a low power 2x2 11a/b/g/n/ac dual-band Wi-Fi subsystem and a Bluetooth subsystem. The Wi-Fi subsystem contains the 802.11a/b/g/n/ac radio, baseband, and MAC that are designed to meet both the low power and high throughput application. MT7663BUN has a 32-bit RISC MCU that handles Wi-Fi and Bluetooth tasks. The Bluetooth subsystem contains the Bluetooth radio, baseband, link controller. It also uses the 32-bit RISC MCU for the Bluetooth protocols.

1.2 Features

1.2.1 Technology and package

- 9x9 QFN 76 pins package

1.2.2 Power management and clock source

- Integrate high efficiency power management unit with single 3.3V power supply input
- MT7663BUN support 40MHz crystal clock with low power operation in idle mode

1.2.3 Platform

- 32-bit RISC MCU for Wi-Fi/Bluetooth protocols
- Embedded SRAM/ROM
- Programmable and multiplexed GPIO pins
- MT7663BUN - USB device fully compliant to USB v3.0 specification

1.2.4 WLAN

- IEEE 802.11 a/b/g/n/ac compliant
- Support 20/40M bandwidth in 2.4G band and 20/40/80M bandwidth in 5G band
- Dual-band 2T2R mode
  - MT7663BUN data rate up to 867Mbps
- Support MU-MIMO RX
- Support STBC, LDPC, TX Beamformer and RX Beamformee
- Greenfield, mixed mode, legacy modes support
- IEEE 802.11 d/e/h/i/j/k/r/v/w support
- Security support for WFA WPA/WPA2/WPA3 personal, WPS2.0
- QoS support of WFA WMM, WMM PS
- Integrated LNA, PA, and T/R switch
- Optional external LNA and PA support.

1.2.5 Bluetooth

- Supports Bluetooth 5 dual mode for 2x the speed
- Integrated BALUN and PA with 13dBm(class 1) transmit power

- RX sensitivity: GFSK -95dBm, DQPSK -94dBm, 8-DPSK -88dBm, BLE1Mbps -98dBm, BLE2Mbps -95dBm, BLR 500Kbps -101dBm, BLR 125Kbps -104dBm
- Supports BT/Wi-Fi coexistence
- Supports 7 BT links and 16 BLE link
- Supports SCO and eSCO link with re-transmission
- Supports wide-band speech
- Supports mSBC and SBC including mono and stereo
- Supports Packet Loss Concealment (PLC) function for better voice quality
- Supports secure connection with AES128 and ECC256
- Channel quality driven data rate adaptation
- Channel assessment and WB RSSI for AFH

1.2.6 Miscellaneous

- Integrate 8Kbit efuse to store device specific information and RF calibration data.
- Advanced FDD/TDD mode Wi-Fi/Bluetooth coexistence scheme

1.3 Block Diagram

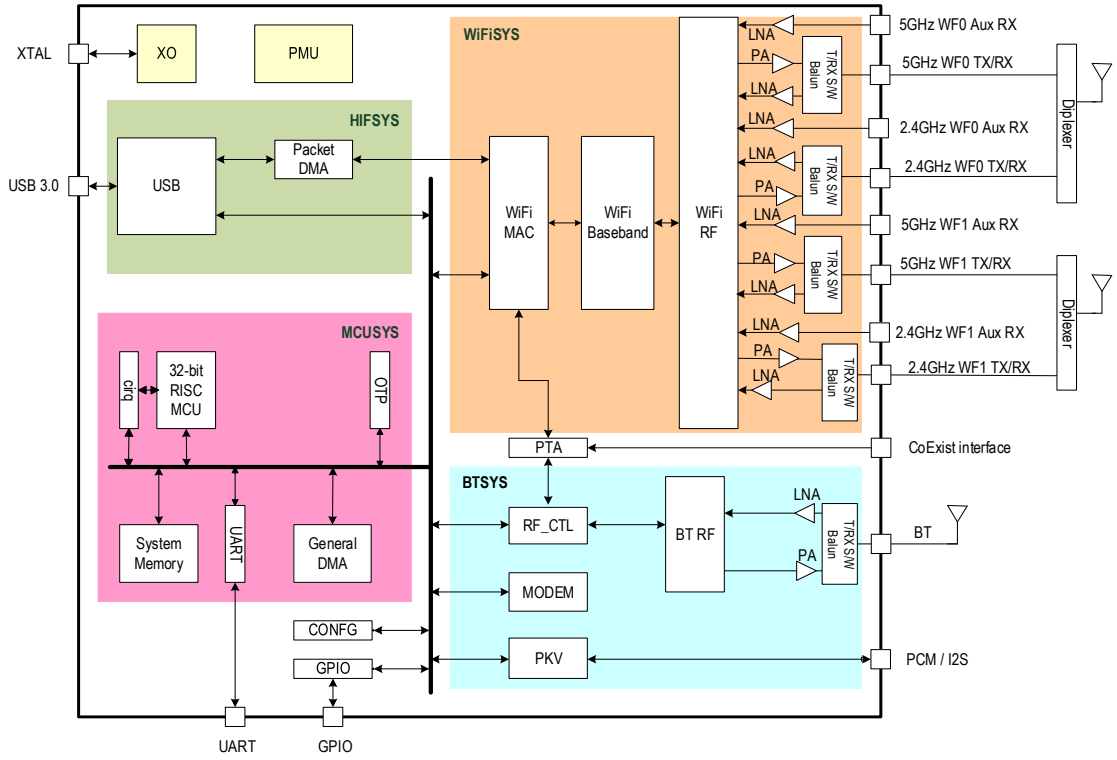


Figure 1 MT7663BUN system-on-chip block diagram

2 Functional Description

2.1 Overview

MT7663BUN is designed to support high data throughput over Wi-Fi. The host interface USB3.0 are integrated to provide stable bandwidth between the host platform and MT7663. The clock rate of the internal bus fabric can also support the throughput the requirement. The clock rate of MCU is also configurable for different kinds of scenarios.

MT7663BUN supports low power requirement. Multiple power domains are implemented on chip. It defines a deep sleep mode, in which only the AON domain is powered on, while other OFF domains are shut off by the power switches integrated on chip. In deep sleep mode, the PMU could be further configured to be in a low power state to save the power consumption. The power, clock, and reset schemes of MT7663BUN are described in 2.2.

MT7663BUN has one CPU subsystem. There is a 32-bit RISC MCU subsystem. The CPU has its local memory. They also have common memory space for MEMORY and memory-mapped hardware engine. There are several options of clock frequency to provide the optimal performance with the best power consumption. The 32-bit RISC MCU is used to do clock control, power management, and host interface configuration. It also handles Wi-Fi MAC operations, and Bluetooth LC operations and audio functions. PDMA (packet DMA) engines are integrated to support on-the-fly data buffer management. The architecture of 32-bit RISC MCU subsystem is described in 2.3.

MT7663BUN features USB3.0 for the host interface. The configuration and the feature set of the interface are described in 2.4.

MT7663BUN has the Wi-Fi MAC, BBP, and the RF subsystems, which provide the best-in-class radio and low power performance. The architecture of Wi-Fi subsystem is described in 2.5.

MT7663BUN has the Bluetooth LC/BB and the RF subsystems. The architecture of Bluetooth subsystem is described in 2.6.

2.2 Chip architecture

The section describes the power, clock, and reset schemes in MT7663.

2.2.1 Chip power plan

The external power source can be directly supplied to the Power Management Unit, digital IOs, USB PHY, and RF circuitry on MT7663. The on-chip Power Management Unit contains 1 switching regulator and a number of LDOs. It converts the 3.3V input to other power rails.
PMU:

- 3.3V to 1.8V by PHYLDO for digital IOs and USB PHY circuit.
- 3.3V to 1.4V by the switching regulator (Buck converter) for CLDO and RF circuit.
- 1.4V to 1.05V by CLDO for digital circuit.

RF:

- 1.4V to lower voltages by the RF LDOs for RF circuits.

2.2.2 Chip power on sequence

The figure below shows the chip power on sequence.

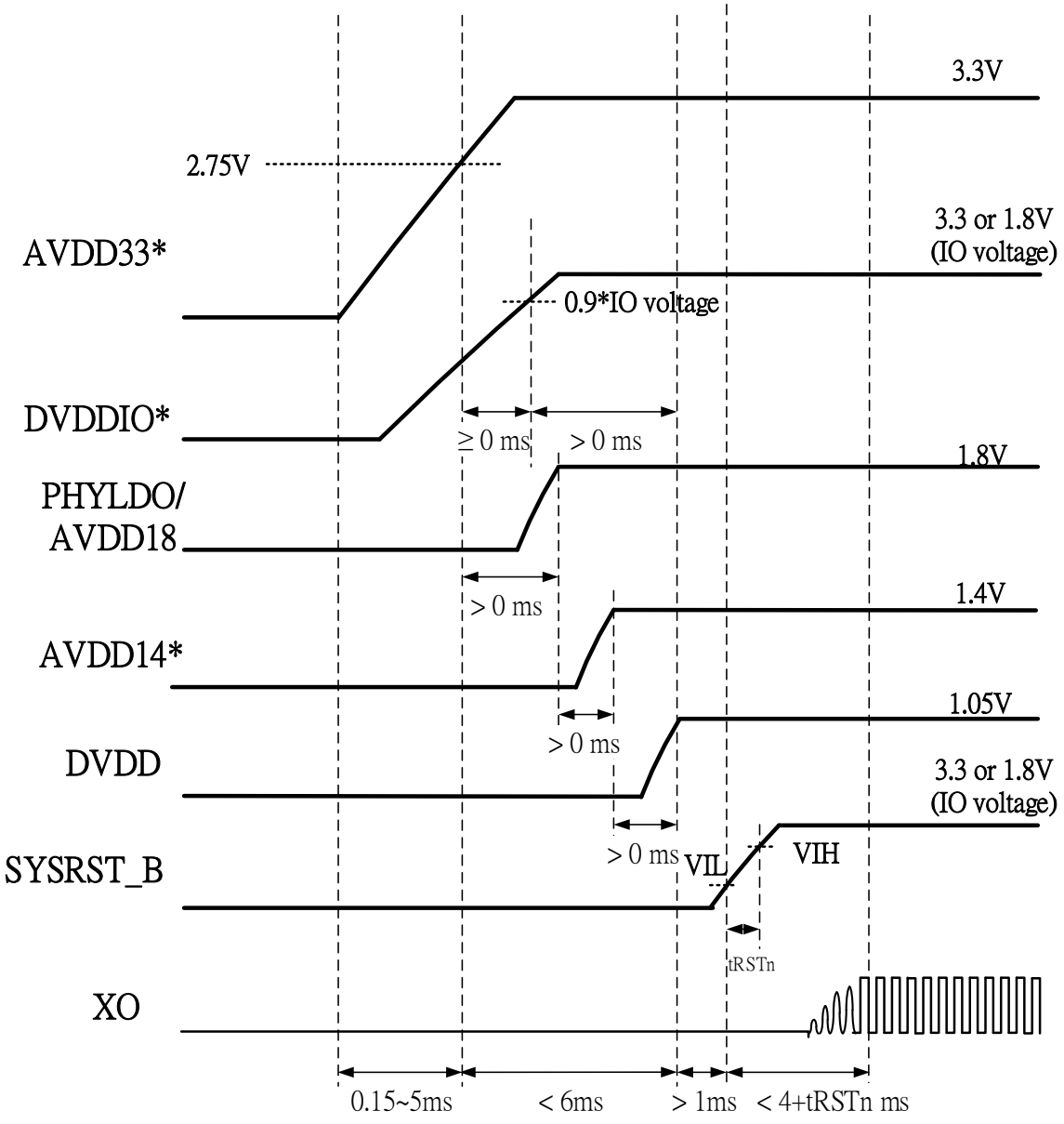


Figure 2 Chip power on sequence

2.2.3 Digital power domain

The digital circuit is separated into AON (always-on), MCU, Wi-Fi MAC, Wi-Fi baseband, Bluetooth, and USB power domains. Except AON, each power domain can be turned off individually for different sleep scenarios.

2.2.4 Clock

2.2.4.1 Clock scheme

MT7663BUN connects to the crystal (XTAL) or the external clock source as the single clock source of the whole system. MT7663BUN XTAL oscillator support 40MHz only.
There are 2 major PLLs, BT PLL, and WF PLL that generate the clocks for the digital circuit. The clocks can be gated to save power when it's not used.

2.2.5 Reset

2.2.5.1 Global reset

MT7663BUN has 2 global resets as follows:

- Cold reset by AVDD33_BUCK, AVDD33_MISC — Whole chip reset.
- System reset by SYSRST_B – Reset digital circuit, include strapping and XTAL controller.

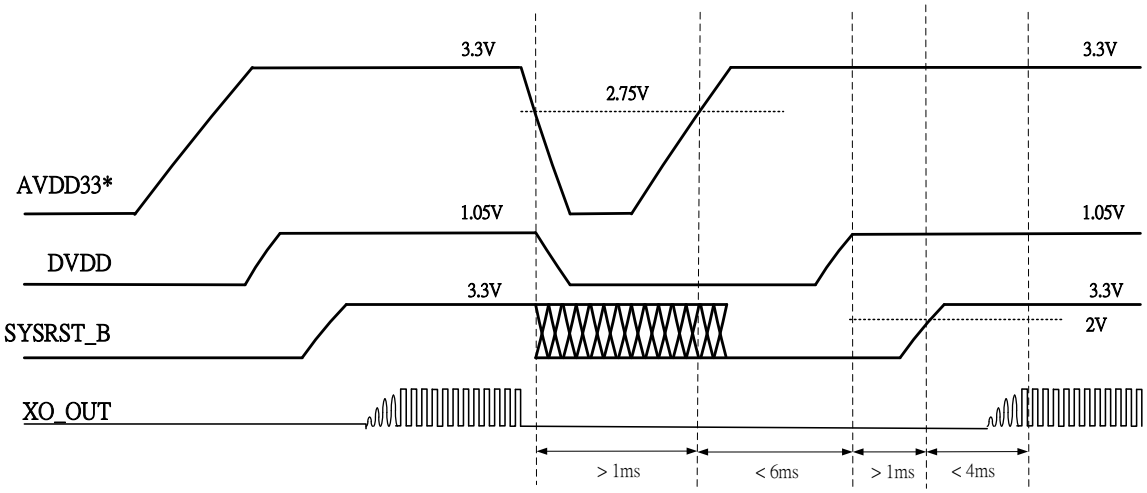


Figure 3 Cold reset sequence

2.3 32-bit RISC MCU subsystem

The 32-bit RISC MCU subsystem is built upon a multi-layer AHB bus fabric infrastructure. There is 880KB ROM and 560KB RAM in local instruction memory, and 368KB RAM in local data memory, with 1T access capability.

2.4 Host interface subsystem

2.4.1 USB Interface

MT7663BUN supports USB device port which is fully compliant with the Universal Serial Bus Specification, Revision v3.0 (USB v3.0 specification). It supports high-speed and full-speed mode, suspend/resume signaling, as well as remote wake-up signaling.

MT7663BUN offers Bluetooth SIG standard HCI interface over USB. It contains the following endpoints:

- A Control Endpoint (Endpoint 0x0) for HCI commands.
- An Interrupt Endpoint (Endpoint 0x81) for HCI events.
- A Bulk IN Endpoint (Endpoint 0x82) for receiving ACL data.
- A Bulk OUT Endpoint (Endpoint 0x02) for transmitting ACL data.
- An Isochronous IN Endpoint (Endpoint 0x83) for receiving SCO/eSCO PCM voice.
- An Isochronous OUT Endpoint (Endpoint 0x03) for transmitting SCO/eSCO PCM voice.

It offers 6 OUT Endpoints (Endpoint 0x04~0x09) and 2 IN Endpoints (Endpoint 0x84~0x85) for Wi-Fi data transmission with flexible queue management.

Data aggregation is used to enhance the throughput over USB interface. Internal pull-up and pull-down resistors are integrated to indicate signaling speed capability. The USB descriptors including VID and PID can be customized. The configuration of the endpoints and the customized USB descriptors are predefined and stored in the Efuse. They are fetched and used by the USB firmware to provide the desired setting.

2.5 Wi-Fi subsystem

2.5.1 Wi-Fi MAC

2.5.1.1 Features

Wi-Fi MAC supports the following features:

- Support all date rates of 802.11a/g including 6, 9, 12, 18, 24, 36, 48, and 54Mbps
- Support short GI and all data rates of 802.11n including MCS0 to MCS15
- Support 802.11ac MCS0 to MCS9
- AMPDU/AMSDU RX (de-aggregation) and TX (aggregation) support
- TX beamformer and RX beamformee
- TX rate adaptation
- TX power control
- Security
  - 64-bit WEP (WEP-40) and 128-bit WEP (WEP-104) encryption with hardware TKIP and CKIP processing
  - AES-CCMP hardware processing
  - GCMP hardware processing
  - SMS4-WPI (WAPI) hardware processing
- Low power beacon filtering
- Management/control frame filtering

2.5.2 WLAN Baseband

2.5.2.1 Features

Wi-Fi baseband supports the following features:

- 20/40/80 MHz channels
- VHT MCS0-9 BW20/40/80MHz with Nss=1~2

- Short Guard Interval
- Space-time block code (STBC)
- Low Density Parity check (LDPC)
- Support digital pre-distortion to enhance PA performance
- Smoothing (channel estimation) extension to MIMO case
- DFS radar detection
- Beamformer (explicit)
  - Decoded BW20/40/80 up to 2x2 BF matrix apply
- Beamformee
  - Decoded BW20/40/80 up to 4x2 MU matrix feedback
- MU-MIMO RX

2.5.3 WLAN RF

RF supports the following features:

- Integrated 2.4GHz/5GHz PA and LNA, and T/R switch
- Integrated 2.4GHz/5GHz Balun
- Support 2.4GHz/5GHz external PA and LNA
- Support frequency band
  - 2400-2497MHz
  - 5150-5350MHz
  - 5470-5725MHz
  - 5725-5850MHz
  - 5850-5925MHz
- Configurable PA that provides different PA modes at different power levels for power consumption optimization

2.6 Bluetooth subsystem

2.6.1 Feature set

MT7663BUN Bluetooth supports the following features:

- Bluetooth 5.1
  - BLE 2Mbps
  - BLE Long Range
  - BLE Advertising Extension
  - BLE high duty cycle non-connectable ADV
  - BLE Channel Selection#2
- Compatible Bluetooth 4.2
  - LE privacy 1.2
  - Data length extension
  - LE security connection
- Single-ended, RF port with integrated Balun and T/R switch
- Integrated high efficiency PA and TSSI

- Baseband and radio BDR and EDR packet types: 1Mbps (GFSK), 2Mbps (π/4-DQPSK), and 3Mbps (8PSK).
- Fully functional Bluetooth baseband: AFH, forward error correction, header error control, access code correlation, CRC, whitening.
- Standard pairing, authentication, link key, and encryption operation.
- Standard power saving mechanisms: sniff mode and sniff-subrating.
- Interlaced scan for faster connection setup
- Up to 7 simultaneous active ACL connections with background inquiry and page scan
- Up to 16 BLE links
- Scatternet support
- Channel quality driven data rate control
- WB RSSI support. Monitor environment air condition to select good channel for AFH

The Bluetooth baseband subsystem of MT7663BUN contains a baseband processor which supports timing control, bit stream processing, encryption, frequency hopping and modulation/demodulation. The baseband processor supports Bluetooth 5 dual mode for 4x the range, 2x the speed and 8x the broadcasting message capacity, and contains the voice codec, PCM interface controller, WLAN coexistence interface controller and a sleep mode controller. It also supports SCO over I2S, and can function as I2S master or slave. The I2S interface signals share the pins of PCM interface. MT7663BUN Bluetooth enhances BT and BLE encryption with AES-128.

One hardware accelerator is added to implement packet loss concealment function. The packet loss concealment (PLC) function is used to improve the voice quality in a noisy environment. Deep sleep mode function and PLL idle mode function are implemented in MT7663BUN to reduce the power consumption in the scan mode.

3 Package specification

3.1 Pin Layout

MT7663BUN uses QFN package of with 9mm x 9mm dimension.

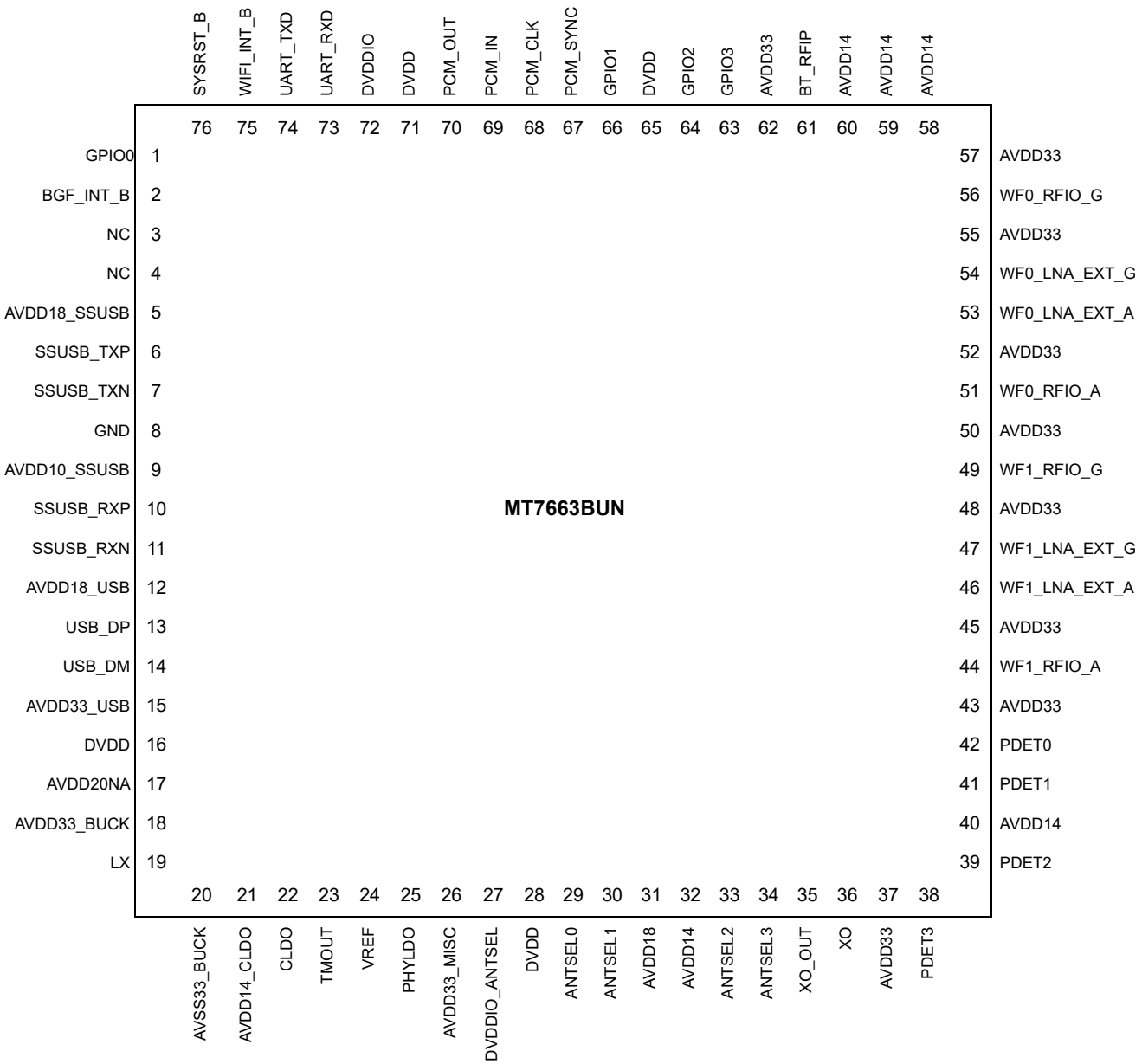
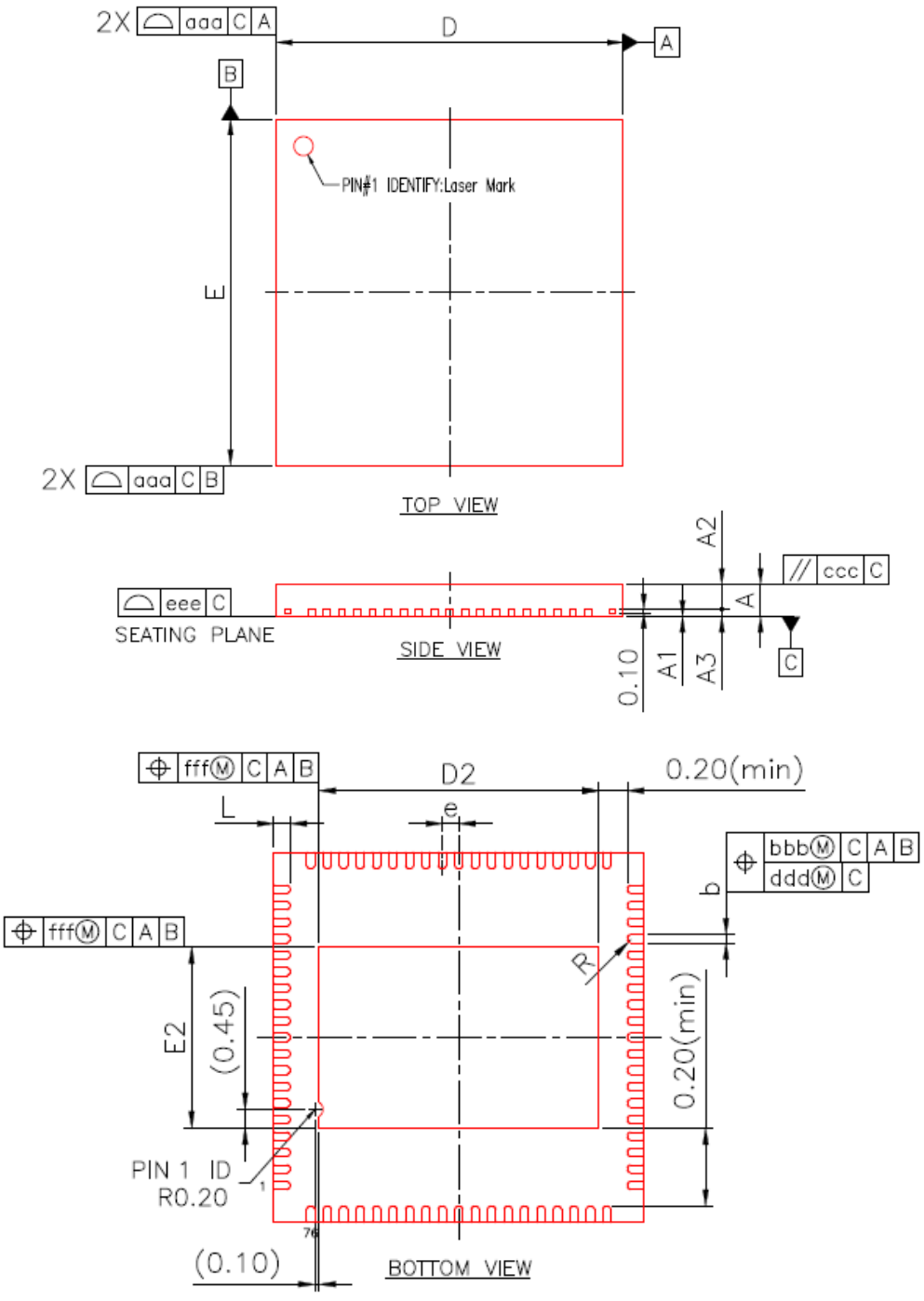


***Figure** 4 MT7663BUN Pin Layout*

3.2 Package information



Item		Symbol	MIN.	NOM.	MAX.
total height		A	0.80	0.85	0.90
stand off		A1	0.00	0.02	0.05
mold thickness		A2	0.60	0.65	0.70
leadframe thickness		A3	0.20 REF.		
lead width		b	0.15	0.20	0.25
package size	X	D	8.90	9.00	9.10
	Y	E	8.90	9.00	9.10
E-PAD size	X	D2	6.70	6.80	6.90
	Y	E2	4.30	4.40	4.50
lead length		L	0.30	0.40	0.50
lead pitch		e	0.40 bsc		
lead arc		R	0.075	---	---
Package profile of a surface		aaa	0.10		
Lead position		bbb	0.07		
Paralleliam		ccc	0.10		
Lead position		ddd	0.05		
Lead profile of a surface		eee	0.08		
Epad position		fff	0.10		

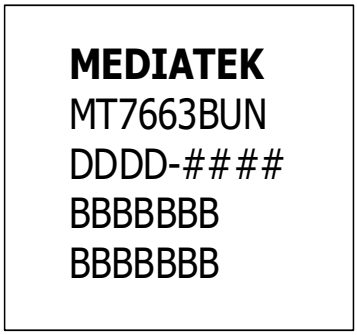
Figure 5 Package outline drawing

3.3 Ordering Information

Part number	Package	Operational temperature range
MT7663BUN	9x9x0.9 mm 76-QFN	-10~70°C

Table 1 Ordering information

3.4 Top marking



MT7663BUN : Part number
DDDD : Date code
: Internal control code
BBBBBBB : Lot number

Figure 6 MT7663BUN Top Marking

ESD CAUTION

MT7663B is ESD (electrostatic discharge) sensitive device and may be damaged with ESD or spike voltage. Although MT7663B is with built-in ESD protection circuitry, please handle with care to avoid the permanent malfunction or the performance degradation.